RADC-TR-72-157
Quarterly Technical Report
March 1972

INVESTIGATION OF 10.6 MICRON PROPAGATION PHENOMENA
Dual Channel Infrared Scanner

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(2880-6)

The Ohio State University

ElectroScience Laboratory

Department of Electrical Engineering
Columbus, Ohio 43212

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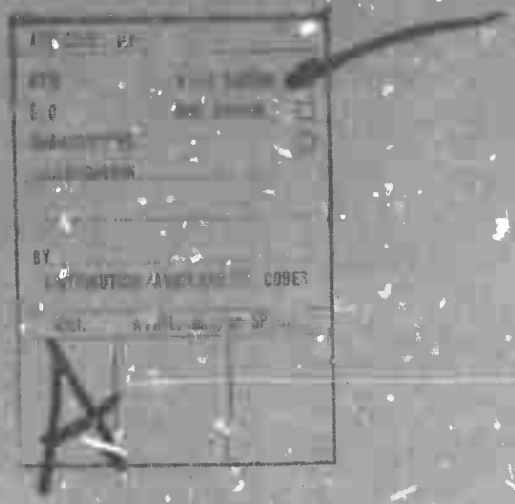

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1. ORIGINATING ACTIVITY *(Corporate author)*
The Ohio State University ElectroScience Laboratory
Department of Electrical Engineering,
Columbus, Ohio 43212

2a. REPORT SECURITY CLASSIFICATION
Unclassified

2b. GROUP

3. REPORT TITLE
INVESTIGATION OF 10.6 MICRON PROPAGATION PHENOMENA

4. DESCRIPTIVE NOTES *(Type of report and inclusive dates)*
Quarterly Report 8 October 1971 to 8 January 1972

5. AUTHOR(S) *(Last name, first name, initial)*
Dr. William G. Swarner

6. REPORT DATE	7a. TOTAL NO. OF PAGES	7b. NO. OF REFS
March 1972	160	23

8a. CONTRACT OR GRANT NO.	9a. ORIGINATOR'S REPORT NUMBER(S)
F30602-70-C-0003 b ARPA Order No. 1279 c. Program Code No. 9E20 d.	ElectroScience Laboratory 2880-6
	9b. OTHER REPORT NO(S) *(Any other numbers that may be assigned this report)* RADC-TR- 72-157

10. AVAILABILITY/LIMITATION NOTICES
Approved for public release; distribution unlimited.

11. SUPPLEMENTARY NOTES	12. SPONSORING MILITARY ACTIVITY
Monitored by: Raymond J. Urtz, Jr. RADC (OCSE), GAFB NY 13440	Advanced Research Projects Agency Arlington, VA 22209

13. ABSTRACT

This report summarizes technical details of work performed at The Ohio State University ElectroScience Laboratory during the period 8 October 1971 to 8 January 1972.

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This system is now ready for delivery to RADC where initial experiments are to be performed in which atmospherically degraded images of a pair of point sources are to be recorded. The resulting data will then be processed at OSU for image restoration and for determination of atmospheric MTF and isoplanatic patch size for various atmospheric conditions.

DD FORM 1 JAN 64 1473

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14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
10.6 Microns Image scanning Atmospheric imaging Image restoration Propagation Turbulence						

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INVESTIGATION OF 10.6 MICRON PROPAGATION PHENOMENA
Dual Channel Infrared Scanner

Dr. William G. Swarner

Contractor: The Ohio State University
ElectroScience Laboratory
Contract Number: F30602-70-C-0003
Effective Date of Contract: 8 July 1969
Contract Expiration Date: 8 July 1972
Amount of Contract: $349,943.00
Program Code Number: 9E20

Principal Investigator: Dr. William G. Swarner
Phone: 614 422-6677

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This research was supported by the Defense Advanced Research Projects Agency of the Department of Defense and was monitored by Raymond P. Urtz, Jr. RADC (OCSE), GAFB, NY 13440 under Contract F30602-70-C-0003.

PUBLICATION REVIEW

This technical report has been reviewed and is approved.

Raymond P. Utz Jr.
RADC Project Engineer

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ILLUSTRATIONS

ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

TABLES

ERRATA

The following are corrections for the present report (2880-6).

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8 Fig. 5
(PROTECTED IMAGE) - PROJECTED IMAGE

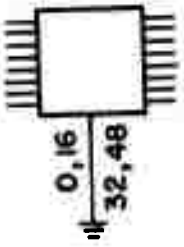
55 11 lines from bottom
(mounted on decoder board) - mounted on encoder board

56 5 lines from bottom
(decoder strobe 1-slot) - decoder strobe 1-shot

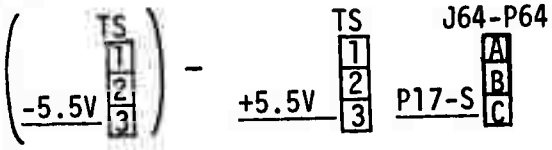
60 27 lines from top
(system clear 1-slot) - system clear 1-shot

81 Fig. 21 -
Box upper left corner

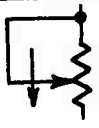
Fig. 21
Box second from left bottom



83 Fig. 22



91 Fig. 30



95 Fig. 34
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1.34μs

I. INTRODUCTION

This is the sixth technical report on Contract No. F30602-70-C-0003 entitled "Investigation of 10.6 Micron Propagation Phenomena," and covers the period 8 October 1971 to 8 January 1972.

This program initially provided theoretical backup to the RADC Atmospheric Optical Propagation Studies Program and is currently centered on the study of atmospheric imaging and restoration of atmospherically degraded images at 10.6 microns. The general aim is to provide initial attempts at restoration, to determine potential problems, and to obtain initial data useful for preliminary systems design. For this purpose an infrared scanning, recording, and display system has been completed and tested which will record, in digital format, two 10.6 micron images simultaneously at 200 frames per second. This system is now ready for shipment to RADC where it is to be used with the RADC 16 inch Boller-Chivens telescope for recording atmospherically degraded laser beams for a variety of propagation paths and atmospheric conditions. The resulting data will be returned to the Ohio State University ElectroScience Laboratory for computer analysis to determine atmospheric MTF and isoplanatic patch size, and to perform experiments in image restoration. A data playback and display system interfaced with the ESL data processing system is currently being implemented for this purpose. Details of the experiments and subsequent data analysis to be performed as well as preliminary data and results obtained during tests of analog portions of the system have been given previously.[1,2,3]

The dual-channel infrared scanning, display, and recording system is fully documented in the remaining chapters of this report. Chapter II contains a general description and specifications for the system, including photographs and block diagrams. Chapter III contains instructions for installation and operation of the system. The theory of operation of each part of the system is given in Chapter IV with reference to the schematic, logic, and timing diagrams of Appendix I. Chapter V is a summary. Appendices II and III give additional details on sync signals required for 2-channel multiplexed operation, and on scanning disc parameters and scanning sequence, respectively; while Appendix IV gives alignment and maintenance instructions.

II. DESCRIPTION AND SPECIFICATIONS

The dual-channel 10.6 micron imaging system (see Fig. 1) consists of three major units, a scanner package designed for mounting to the RADC 16-inch Boller-Chivens telescope (or other suitable primary optics), a control console containing a complete set of remote controls for the scanner together with video and sync circuitry, encoders, decoders and display units, and a magnetic tape recorder. The system is basically a two-channel high speed TV-type scanning system operating at 10.6 microns, with provisions for magnetic tape recording and playback, and visual CRT display of the received infrared images. System

Fig. 1. Photograph of the 10.6 micron imaging system.

specifications are summarized in Table I, and a block diagram of the system is given in Fig. 2 which should be used in conjunction with the following description of overall system operation.

A. Scanner System

At the upper left of Fig. 2 is depicted the basic experiment for which the system is designed although it can be used equally well for any application requiring the reception, recording, and display of one or two simultaneous time-varying infrared images within the capabilities of the system (see Table I). For the experiment shown, the output of a 10.6 micron laser is split into two beams which propagate through the atmosphere and are imaged, as two atmospherically degraded Airy disc patterns, at the image plane of the primary receiving optics. Here the images are separated by means of two movable corner reflectors (see Fig. 3 for details) and are refocused by suitable magnifying and positioning optics onto opposite sides of the scanning disc.

A functional view of the optical system for Channel B of the system is given in Fig. 4. The optical system for Channel A is located to the left of a vertical plane containing the scanning disc axis and is the mirror image of that shown. All optical components of the system except for the field lenses are gold-coated reflective, hence by changing detectors and field lenses the scanner may be used at other wavelengths if desired. Magnifications of 1, 2, and 4 may be remotely selected via stepping motor control, while additional stepping motors are provided for vertical and horizontal image positioning, translation of the image separator corner reflectors, and for inserting cross-hair alignment targets into the optical path. Additional details of the optical system have been given previously.[3,4]

The scanning disc contains two identical sets of scanning apertures so that two images focused on opposite sides of the disc may be scanned simultaneously. The disc rotates at 6000 RPM and scans two complete frames per revolution providing a scanning rate of 200 frames per second for each image. The scanning format used is illustrated in Fig. 5 with respect to an ideal square image to be scanned projected onto the disc. Although vertically scanned lines are slightly curved because of the fixed radii of the scanning apertures, all scanning lines are of equal length so that horizontal lines in the scanned image are preserved and image distortion caused by the scanning process is minimized. Note that linear and angular dimensions are exaggerated in Fig. 5 for purposes of illustration, consequently distortion introduced by the actual system is even less than that shown.

Energy from each image passing through the scanning disc apertures is collected by a field lens and converted to an analog video signal by a nitrogen cooled Cd Hg Te detector. The signal is first amplified by a Perry model 604 preamplifier, which also includes a thermally protected bias circuit for the detector, and is then amplified by variable gain video amplifiers and applied via a channel selector switch as intensity

TABLE I
SCANNING DETECTOR SPECIFICATIONS

Primary Optics	RADC Boller Chivens Telescope (Reflective)
Aperture	40 cm
$f^{\#}$	18
Secondary Optics	Gold coated reflective (off axis parabolas)
Magnification	1, 2, or 4 (externally selectable)
Image Channels	2
Frame Rate	200 frames/sec
Resolution	40 x 40 elements
Image Size	8 mm x 8 mm
Scanning Aperture Dia.	0.2 mm
Disc Radius	12.7 cm
Rotation Speed	6000 RPM
Detector Type	Cd Hg Te
Detector Area	6 mm^2
D* (at 10.6 microns)	10^{10} cm $Hz^{\frac{1}{2}}$ W^{-1}
S/N for 2 mw Incident Power	
Diffraction Limited Spot	≈50 dB
Turbulence Degraded Spot	≈30 dB
Power Requirements:	
Control Console	120 v., 60 Hz. 1 phase, 15 amps. max.
Scanner Unit	120 v., 60 Hz, 1 phase, 10 amps. max, and 120/208 v., 400 Hz (±5%), 3 phase, 3 amps.
Recorder (Ampex FR 1400)	120 v., 60 Hz, 1 phase
Dry Nitrogen for Detector Cooling:	1000-1500 psi
Magnetic Tape	Scotch Cat. No. 888-½-9200 IR, or equivalent

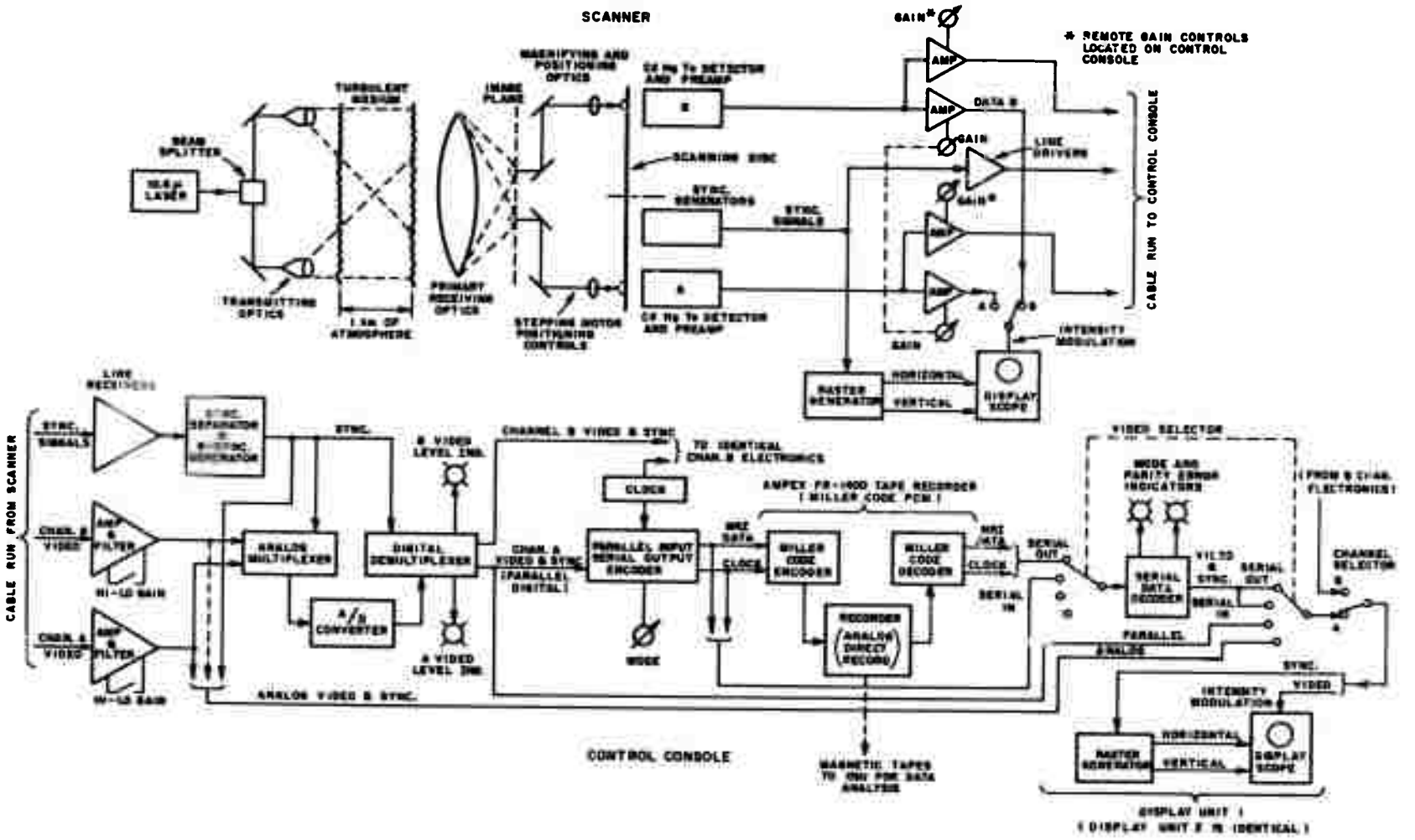


Fig. 2. Block diagram of the 10.6 micron imaging system.

modulation for the scanner mounted display scope. Additional video amplifiers, with remote gain controls located in the control console, are used as video line drivers for approximately 100 ft. of 93 ohm coaxial cable used to conduct the video signals to the control console.

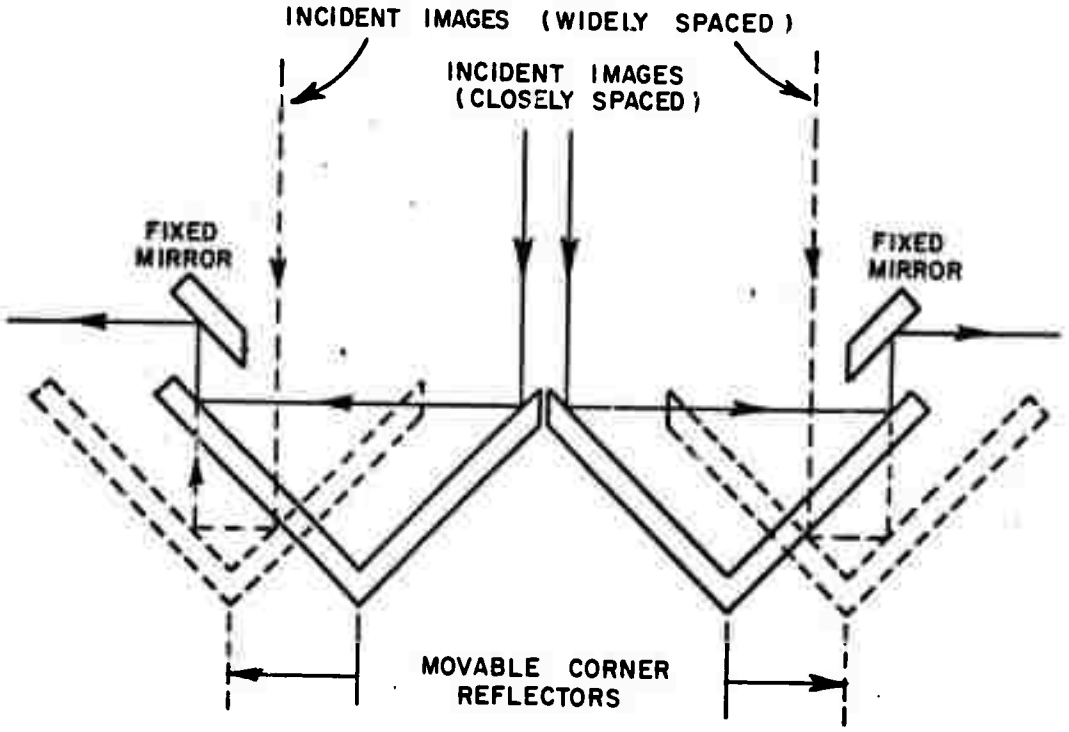


Fig. 3. Image separator.

Synchronizing signals for controlling the digitization of the video signals prior to recording and for generating a raster for reconstruction and visual display of the scanned images are produced by the sync generators of Fig. 2. Additional details of the synchronization system are shown in Fig. 6 and have been described previously.[3,5]

Word sync is generated by projecting two 20-line reticles onto the disc so that they will be scanned by the same set of apertures used to scan the infrared images. Light from these reticles passing through the scanning apertures produce pulses in the outputs of the even and odd word sync photomultiplier detectors which are then sharpened, shortened, and combined to form the channel A word sync pulse train. Channel B word sync is then obtained from Channel A word sync via a delay equal to one half the word spacing of the shortest (outermost) raster line.

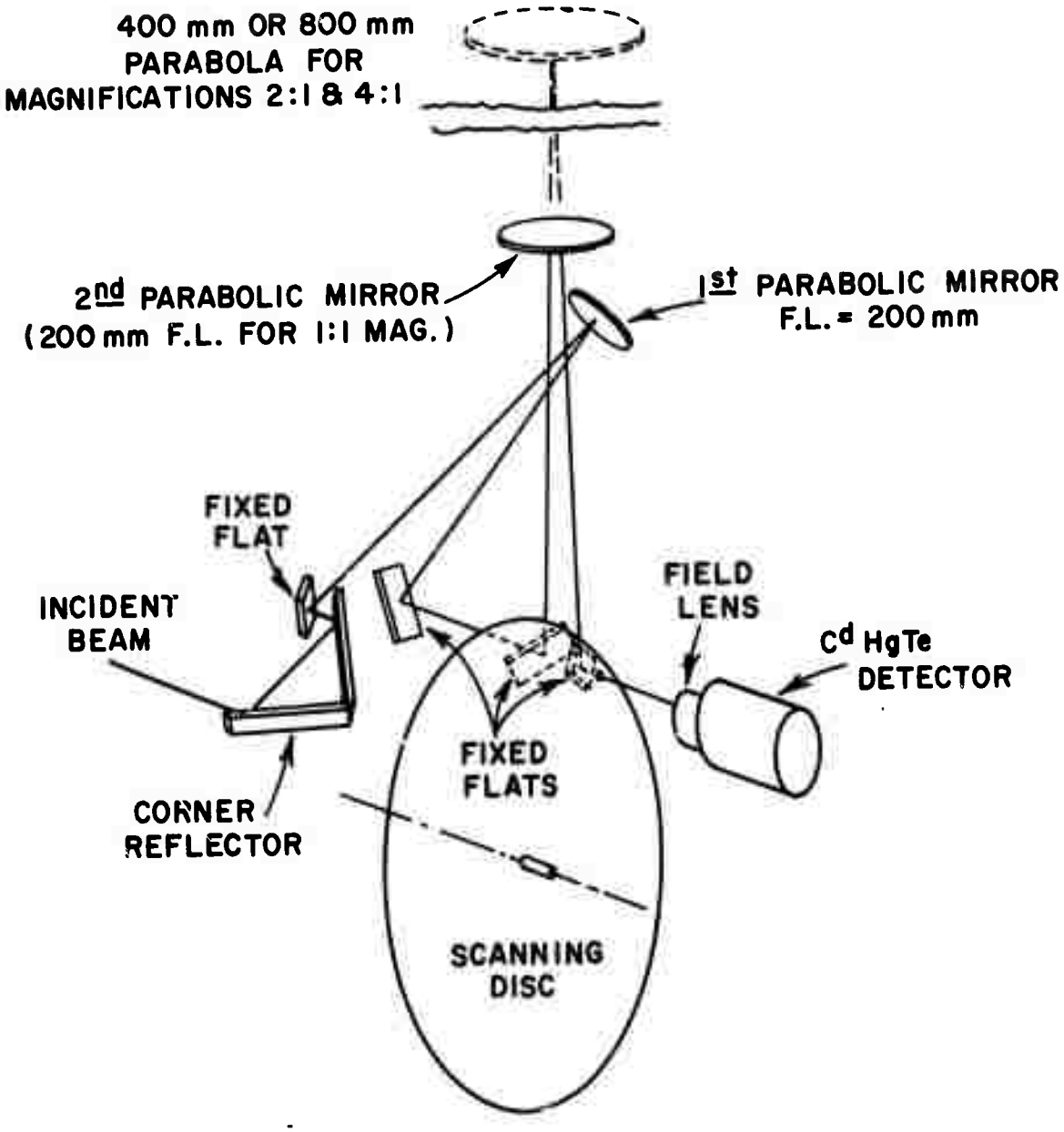


Fig. 4. Functional view of the Channel B optical system.

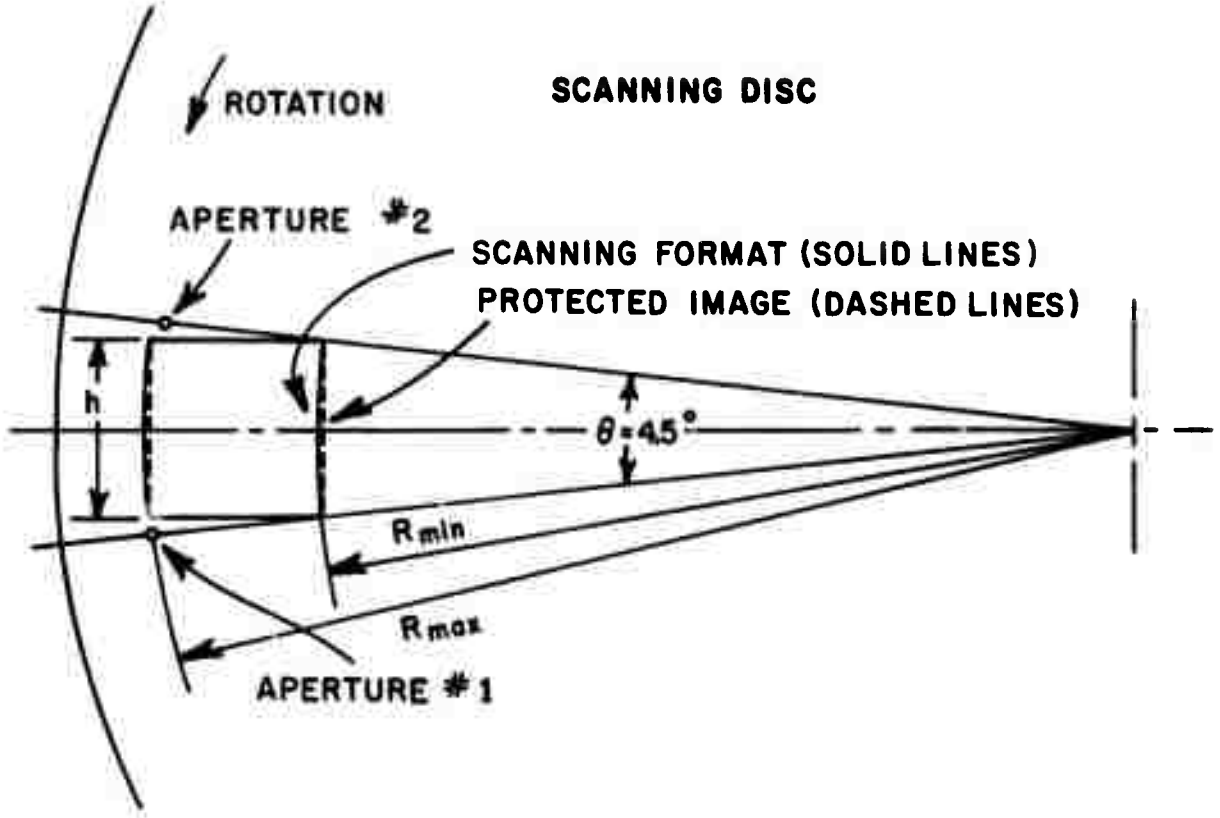


Fig. 5. Scanning format.

Line, frame, and disc sync. pulses are generated similarly by a 3-line projected reticle and photomultiplier operating in conjunction with the scanning apertures (for line sync) and three additional apertures (for frame and disc sync) located near the edge of the scanning disc. Since line, frame and disc sync are all generated by the same detector they appear multiplexed at the detector output and must be separated before use. This is accomplished by suitable logic circuits (see sync separator, Chapter IV).

Word sync, line sync, and frame sync signals are then applied to the raster generator which generates a digital x-y raster for visual display of the received video image on the scanner-mounted display scope. The Channel A word sync pulse train and the multiplexed line, frame, and disc sync pulse train are each applied to digital line drivers and transmitted via 100 ft. 93 ohm coaxial cables to the control console.

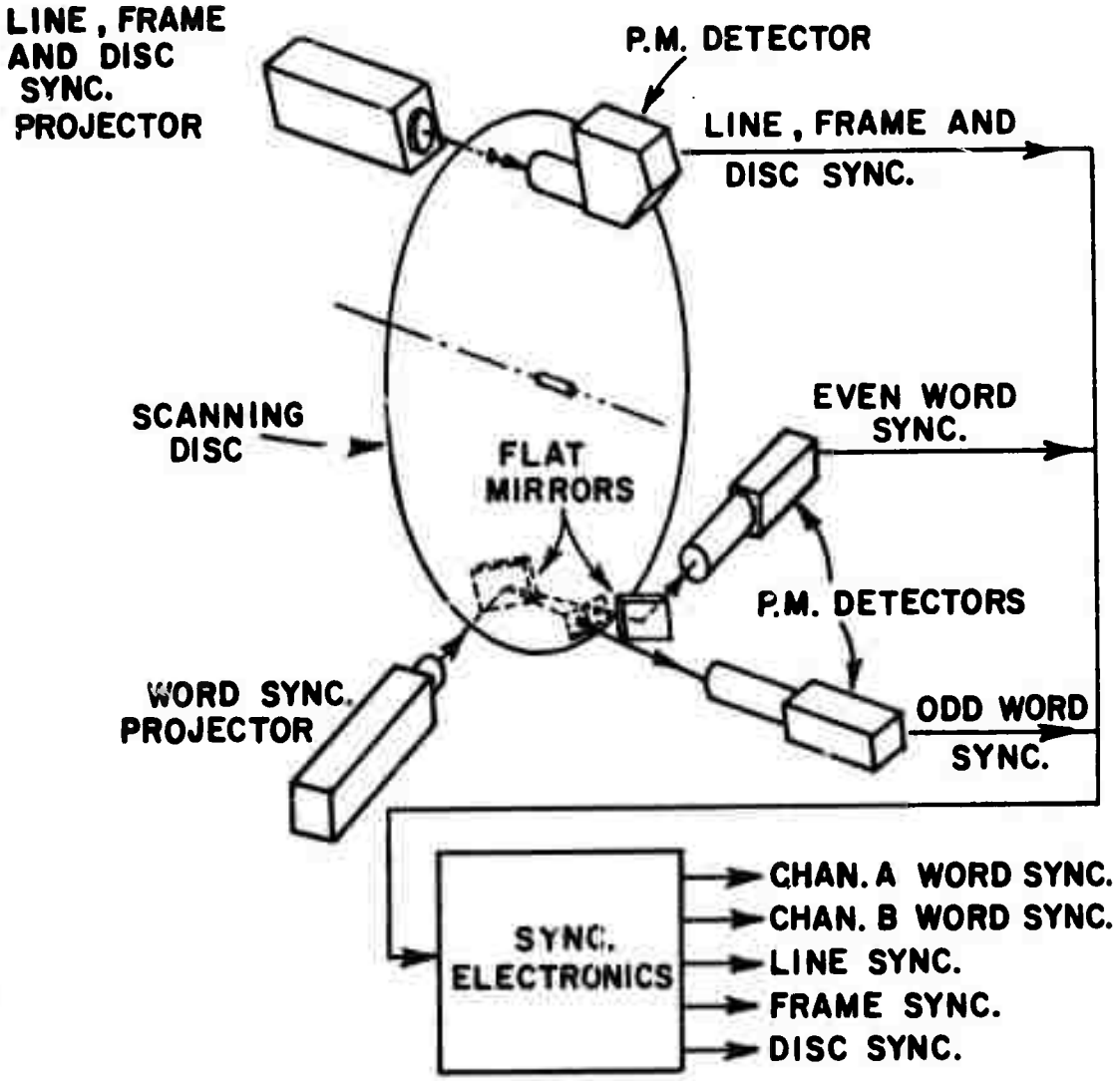


Fig. 6. Scanner synchronization system.

B. Control Console, Recorder, and Display

Sync signals from the scanner are applied to line receivers in the control console and then to the sync separator and B-sync generator which provide separate output signals for Channel A and Channel B word sync, line sync, frame sync, and disc sync for use throughout the console as shown in Fig. 2.

The channel A and Channel B video signals arriving at the console from the scanner are separately amplified and matched to low-pass filters which eliminate excess noise outside the passband of the video signals prior to sampling. These amplifiers have hi-lo gain switches which, together with the console mounted gain controls for the video amplifiers in the scanner, permit the video levels to be set for optimum utilization of the analog-to-digital conversion capability of the system. The video signals are then multiplexed so that a single A/D converter may be used for both channels, and are sampled and digitized to 8-bit accuracy. They are then separated by the digital demultiplexer which supplies separate A channel and B channel video in parallel digital form (i.e., on 8 parallel data lines) to the remaining circuitry which, except for a common clock, is essentially duplicated for the two channels. The digital demultiplexer also drives A channel and B channel video level indicators which indicate full scale output from the A/D converter and thus permit the video gain controls mentioned above to be properly adjusted.

Recording digital data on parallel tracks of magnetic tape at the required data rate is not feasible at present because the dynamic skew between data tracks of state-of-the-art recorders would be greater than the bit spacing. Consequently, a serial digital recording technique which has recently been developed and is capable of handling the required data rate on a single track of an instrumentation tape recorder is used.[6] This technique utilizes the Miller code to eliminate the requirement for dc response, to match the spectral density of the signal to that provided by a conventional direct-record channel, and to permit extraction of a data clock for decoding from the recorded data.

For use with this system, the parallel digital output of the A/D converter must be changed to serial form and the sync pulses required for reconstructing the image upon playback must be inserted into the serial data stream since dynamic skew limitations do not permit these to be recorded on a separate channel. The sync pulses must be uniquely coded so that they may be extracted from the video data at playback. These tasks are accomplished by the parallel input serial output encoder of Fig. 2.

If samples were taken at equal time intervals the scanning lines would be of unequal length since the scanning disc apertures at different radii sweep out equal angles (θ) rather than equal length (h) in a given time (see Fig. 5). To obtain scanning lines of equal length different sampling intervals must therefore be used for each image line. Thus the data samples from the A/D converter are asychronous with respect to a fixed-frequency clock, but since the Miller code recording technique works best with synchronous data the encoder contains sufficient temporary storage and an appropriate clocking system to convert the asynchronous parallel input to a synchronous serial output together with a data clock required by the Miller code system.

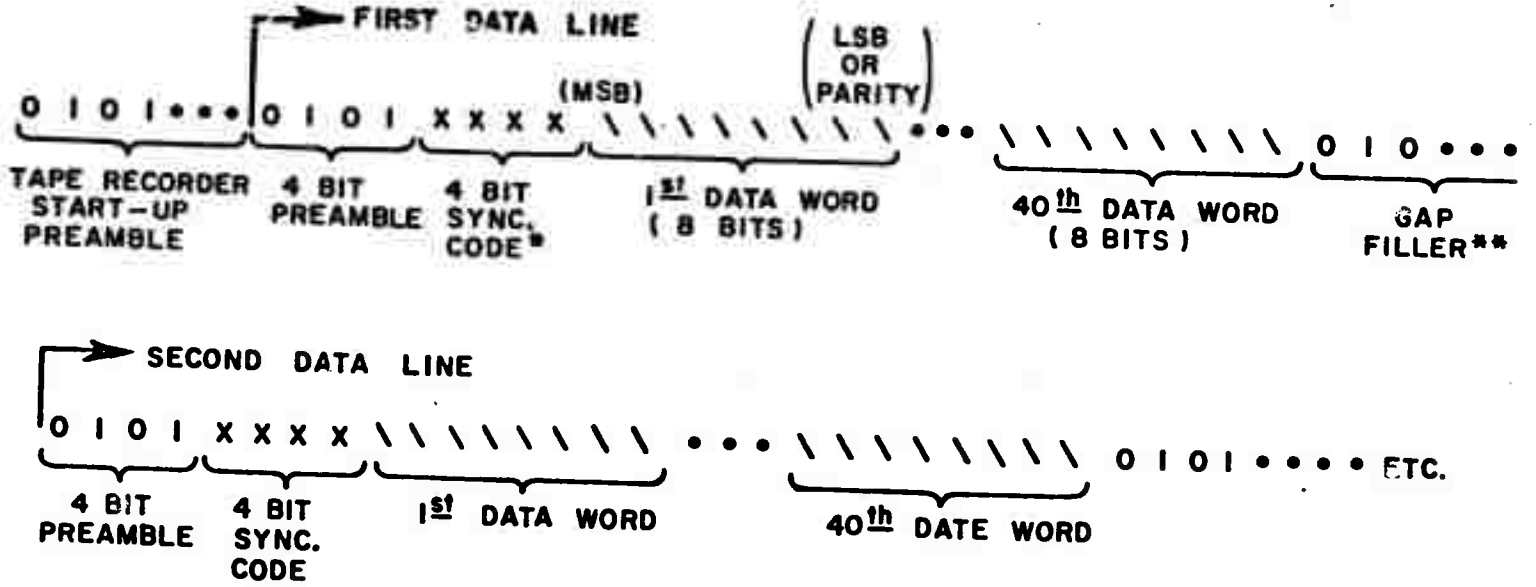
Since the high density (22.6 K bits/in.) recording system used has a non-zero (approximately 1 in 10^6) error probability which could deteriorate with misalignment, dirty, magnetized, or worn recording or reproduce heads, dirty or defective tape, or other reasons, it may be desirable to check the error rate from time to time. For this purpose a mode selector has been provided which permits recording either 8 data bits per word or 7 data bits plus parity. The encoder substitutes a parity check bit for the least significant data bit when the parity mode is selected and also modifies the code used for frame sync so that the mode used during recording can be automatically determined by the decoder during playback of the data tape.

Details of the serial coding technique used and of the Miller code are illustrated by Figs. 7 and 8, respectively, and have been discussed previously.[5,6]

The serial binary NRZ (non-return to zero) data stream and the data clock from the parallel input serial output encoder are applied (via drivers and 93 ohm coaxial cables not shown in Fig. 2) to the Miller code encoder which is located inside the Ampex FR 1400 tape recorder. The output of this encoder is then recorded at 120 ips tape speed on a single direct record channel as mentioned above. In addition to the two recorded data tracks (Channel B is separate from, but identical to, channel A described above --- see Fig. 2) a 200 KHz sinusoidal synchronizing signal supplied by a crystal oscillator (installed in the tape recorder Miller code electronics card cage) is also recorded on a third track. This signal permits tape speed servo control to be used when a tape recorded on this system (normally located at RADC) is played back on a second recorder (to be located at OSU for data analysis) thus eliminating errors which could otherwise be introduced by variations in tape speed between recording and playback.

A remote control panel (not shown in Fig. 2) is included in the control console so that the recorder may be operated from the console. Relays in this panel furnish record and playback off/on logic signals needed by the encoders and decoders.

During playback, the Miller code decoder located in the recorder extracts the data clock from the recorded data, converts the Miller coded data to NRZ binary form, and sends these signals via drivers and 93 ohm coaxial cable to the serial data decoder located in the control console. This decoder extracts frame, line, and word sync pulses from the serial data stream, converts the serial data to parallel digital form, determines what recording mode has been used, and, if the parity check mode was used, provides a signal to illuminate the parity mode indicator and activate the parity checker which is incorporated in the decoder. Each time a parity error is detected an output pulse is generated causing the parity error indicator to blink thus giving a visual indication of the presence and relative rate of occurrence of errors introduced during the recording or playback process.



* SYNC CODES

0000 = LINE SYNC

0011 = FRAME SYNC., 8 DATA BIT MODE

1100 = FRAME SYNC., 7 BIT + PARITY MODE

** GAP FILLER = AN EVEN NO. OF 0101•••BITS (NORMALLY 10 TO 12 BITS)

Fig. 7. Serial coding technique.

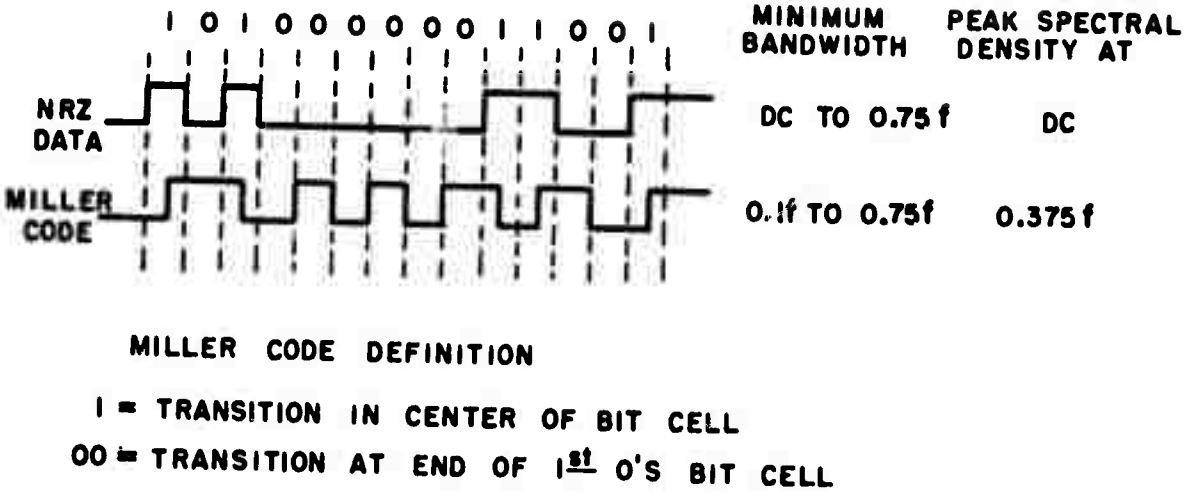


Fig. 8. Miller code format.

Word, line, and frame sync pulses are applied to a raster generator which generates a digital x-y raster for the console display scope, while the video signal from the decoder is applied (via a buffer and digital-to-analog converter not shown in Fig. 2) to intensity modulate the display scope thus providing a visual display of the recorded infrared image.

As indicated by the symbolic switching arrangement in Fig. 2 the display system incorporated in the control console is quite versatile. It may be used to view the output from magnetic tape (Serial Out) as described above either during recording or from a prerecorded tape, the input to the recorder (Serial In), the parallel video signal from the demultiplexer (Parallel), or the analog video similar to that displayed by the scanner display scope (Analog) for either A or B channel as desired. Two identical display systems are provided (except for the second display scope which is to be supplied by RADC) so that video from both channels may be viewed simultaneously or, if desired, video signals from a single channel may be viewed simultaneously during recording at two different points along the signal path.

It should be noted that since the RADC system playback capability is required only for previewing the data and not for data analysis, certain compromises were made (in order to reduce system cost) which result in a higher average error rate for tape reproduction performed on the RADC system as compared to that performed on the OSU system to be used for data analysis. Specifically, a tape recorder with reduced high frequency response has been used and the tape speed servo option has not been included in the RADC system. This in no way degrades the performance of the system for data recording which is the primary function of this system. However, if the system should later be used

for data analysis, it is recommended that the tape recorder be replaced with one more suitable for the reproduction of Miller code data tapes.

III. INSTALLATION AND OPERATING PROCEDURE

A. Installation

System installation consists essentially of mounting the scanner to the telescope which serves as the primary receiving optics; installing the control console components (furnished rack mounted) in the RADC main control console, if desired; supplying primary power to the scanner, control console, and recorder; supplying high pressure dry nitrogen for detector cooling to the scanner; and interconnecting the scanner, control console, and recorder as described below.

1. Control Console

The control console components may be used rack mounted and connected as supplied, or they can be removed from the rack and remounted in the RADC control console. A suggested mounting arrangement for this purpose is given in Fig. 9. All cables and connectors are labeled so that no difficulty should be experienced in reconnecting the units after mounting in the control console. If the logic power supply is mounted below the desk top as suggested, a multiple-outlet power cord (not supplied) plugged into one of the ac outlets on the rear of the power supply chassis should be run to the upper bay to supply power to the multiplexer, D/A converter, and display scope(s) so that power to these units will be controlled by the main power push buttons on the control unit panel.

A second display scope (Hewlett-Packard Model 1330A - to be supplied by RADC) is to be mounted in the space, now covered by a blank panel, to the right of the display scope furnished. Since the video signals supplied to the display scopes are of negative polarity (for increased brightness) it will be necessary to remove the bottom cover plate of the new display scope and reverse the z-axis input leads at the jumper connections to the PC board as shown in the manual supplied with the unit.[7] It may also be desirable to check raster size after the system is put into operation and adjust the x and y gain controls if required before replacing the bottom cover. Cables for supplying x, y, and z axis inputs for the second display scope are coiled inside the rear of the present equipment rack. They should be connected to the second display scope as labeled.

All power for control console components is supplied via the logic unit power supply power cord. This should be connected to a suitable 120 volt, single phase 60 Hz ac power outlet (with power ground) capable of supplying 15 amperes.

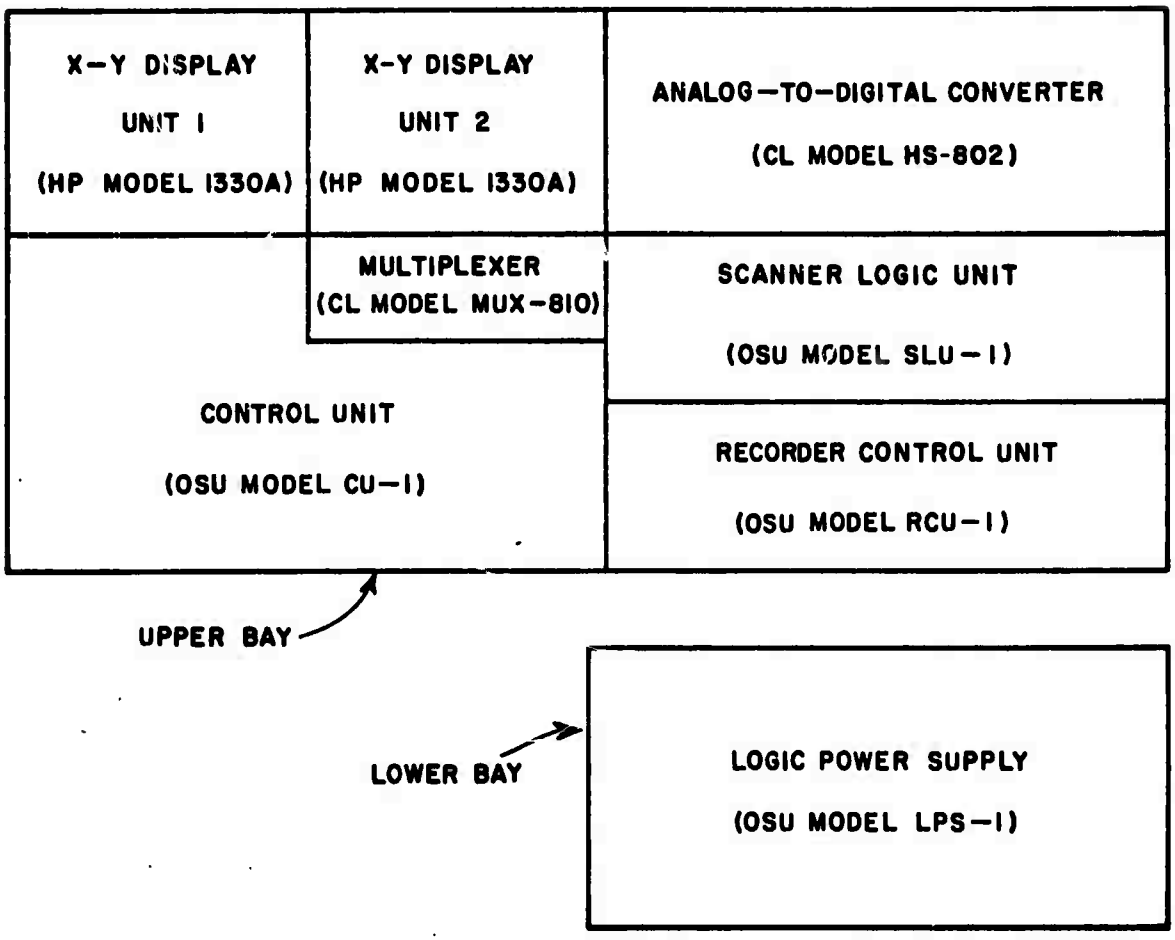


Fig. 9. Equipment mounting arrangement for RADC console.

Interconnections to the magnetic tape recorder consist of 8 93-ohm coaxial cables from the scanner logic unit (card cage) and one remote control cable from the Recorder Control Unit. Cables of approximately 15 ft. length are supplied for this purpose and their use is recommended although longer cables could probably be used without difficulty if required. The cables supplied are appropriately labeled and mate with connectors bearing the same number on the rear of the recorder.

Interconnections with the scanner consist of 4 93-ohm coaxial cables from the scanner logic unit and one control cable from the control unit. Four properly labeled 100 ft. coaxial cables are supplied for interconnection to the scanner. If it is necessary to change the length (or type) of these cables the output line capacitors on the scanner control unit line driver board and the input line capacitors on the scanner logic unit line receiver board should also be changed to values which are equal to the total distributed capacity of the interconnecting

cables. (See Chapter IV and the schematic diagrams of Appendix I for further details.) A control cable of approximately 15 ft. length is also supplied with the system for test purposes. A similar cable of suitable length is to be fabricated and installed by RADC prior to installation of the system. This cable may be Belden #8750, or any other similar, or heavier, cable having a minimum of 52 conductors. An MS 3106A 36-404P connector (P12) is required at the control console (control unit CU-1) and an MS 3106A 36-404S connector (J14) is required at the scanner (control unit CU-2), connected pin for pin. Although no problems with hum pickup are expected, if such should be evident following installation, due to inefficient grounding of the power system and building structure, a heavy ground buss between the control console and scanner may be required. (A ground is included (pin 1) in the control cable, however a larger, lower impedance conductor might be required if hum problems are encountered.)

2. Magnetic Tape Recorder

The magnetic tape recorder should be located where stable temperature and humidity conditions can be maintained and, if possible, within 10 to 15 feet of the control console. The line cord should be connected to a suitable 120 volt, 60 Hz ac power outlet (grounded type) and interconnecting cables from the control console (see above) should be connected to jacks on the rear of the recorder bearing the same numbers as those on the interconnecting cables.

3. Scanner

The scanner is designed for direct mounting to the RADC 16-inch Boller-Chivens telescope. Four mounting studs and three kinematic mounts are provided on the front of the scanner for this purpose (see Fig. 10). A set of shims is included behind each of the two lower kinematic mounts. These should be removed as required (by first loosening the 6-32 socket-head set screws holding the mount pads in place and removing the pads from the mounting blocks) during initial installation so that the optical axis of the telescope is perpendicular to the scanner package mounting plate. The mounting studs should then be tightened using a 5/8 inch end wrench applied to the hexagonal shank of each stud, drawing all studs down evenly to seat the kinematic mounts and clamp the scanner firmly to the telescope. Since the scanner is quite heavy, additional support beneath the scanner package attached to the telescope mount should be supplied to avoid undue strain on the telescope housing, scanner, or kinematic mounts. Two hoisting rings are supplied at the top of the scanner for lifting the unit.

Interconnections with the control console require 4 coaxial cables and one control cable as described above in paragraph 1. These mate with correspondingly numbered connectors located on the bottom plate of the Scanner Control Unit (see Fig. 10). Two additional connectors are provided for primary power input to the

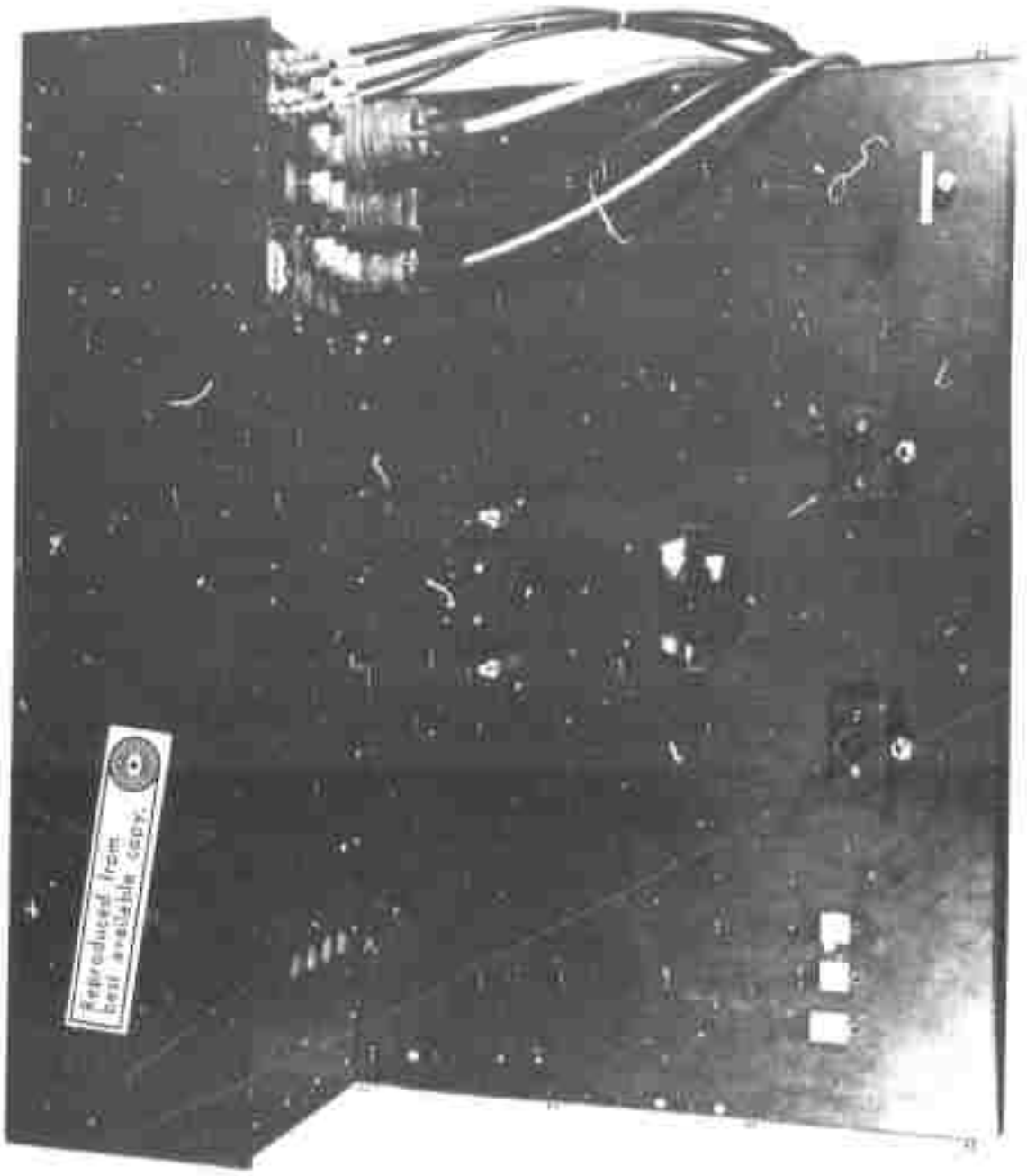


Fig. 10. Scanner mounting and input connectors.

scanner. The cables supplied may be used, or longer ones may be substituted if necessary. The 120 volt, 60 Hz AC power cord (J16) may be connected to any suitable power outlet (grounded type) capable of supplying 10 amperes. The 120/208 volt, 400 Hz, 3 phase power cable (J18) should be connected to a suitable source capable of supplying at least 3 amperes. Frequency of this source must be accurate within ±5% for proper system operation, and voltage should not be lower than approximately 117 volts (line-to-neutral) at the scanner package.

Following initial connection of the 400 Hz power source, the scanner motor must be checked for proper direction of rotation as follows. If the scanner has not been mounted to the telescope the direction of disc rotation can be observed through the front aperture of the scanner housing; otherwise, remove the rear cover plate of the scanner housing. A portion of the disk can then be seen through an aperture near the top of the motor mounting plate behind the line, frame, and disc sync projector. With scanner interconnected with the control console as described above apply power to the control console by pressing the console main power ON pushbutton. (Switch on the front panel of the Logic Power Supply must be in REMOTE position.) The scanner motor may then be turned on to check the direction of rotation by pressing the 400 cycle power ON button on either the control console (CU-1) or scanner (CU-2). Disc rotation must be downward on the A-channel side of the scanner (left side as viewed from the rear of the scanner); otherwise, the sequence of sync pulses will be incorrect and proper operation cannot be obtained. The direction of disc rotation can best be observed as the motor is being started, or is coasting to a stop. If the direction of rotation is incorrect reverse any two phases of the 3 phase input at the point of connection to the 3 phase, 400 Hz power source.

A source of clean, dry nitrogen with regulated pressure variable from 1000 Psi to 1500 psi must be supplied for detector cooling. A standard 1/4 inch OD stainless steel compression fitting (swage lock) is provided on the scanner mounting plate (see Fig. 10) for connection to the nitrogen supply.

B. Operation

1. Controls and Indicators

All controls required for normal operation of the system (other than the recorder) are located on the front panel of the console control unit, CU-1, (see Fig. 11). These controls and their functions are summarized in Table II which also lists the various indicators found on the control unit, and their functions. Several auxiliary controls are available elsewhere on the console but these require infrequent adjustment, or are to be left in a given position for normal system operation. These controls, together with their locations and functions are listed in Table III. The test switch located on the D/A converter (see Table III) may be used to check for proper operation of this unit. Readouts which should be obtained during these tests are listed in Table IV.

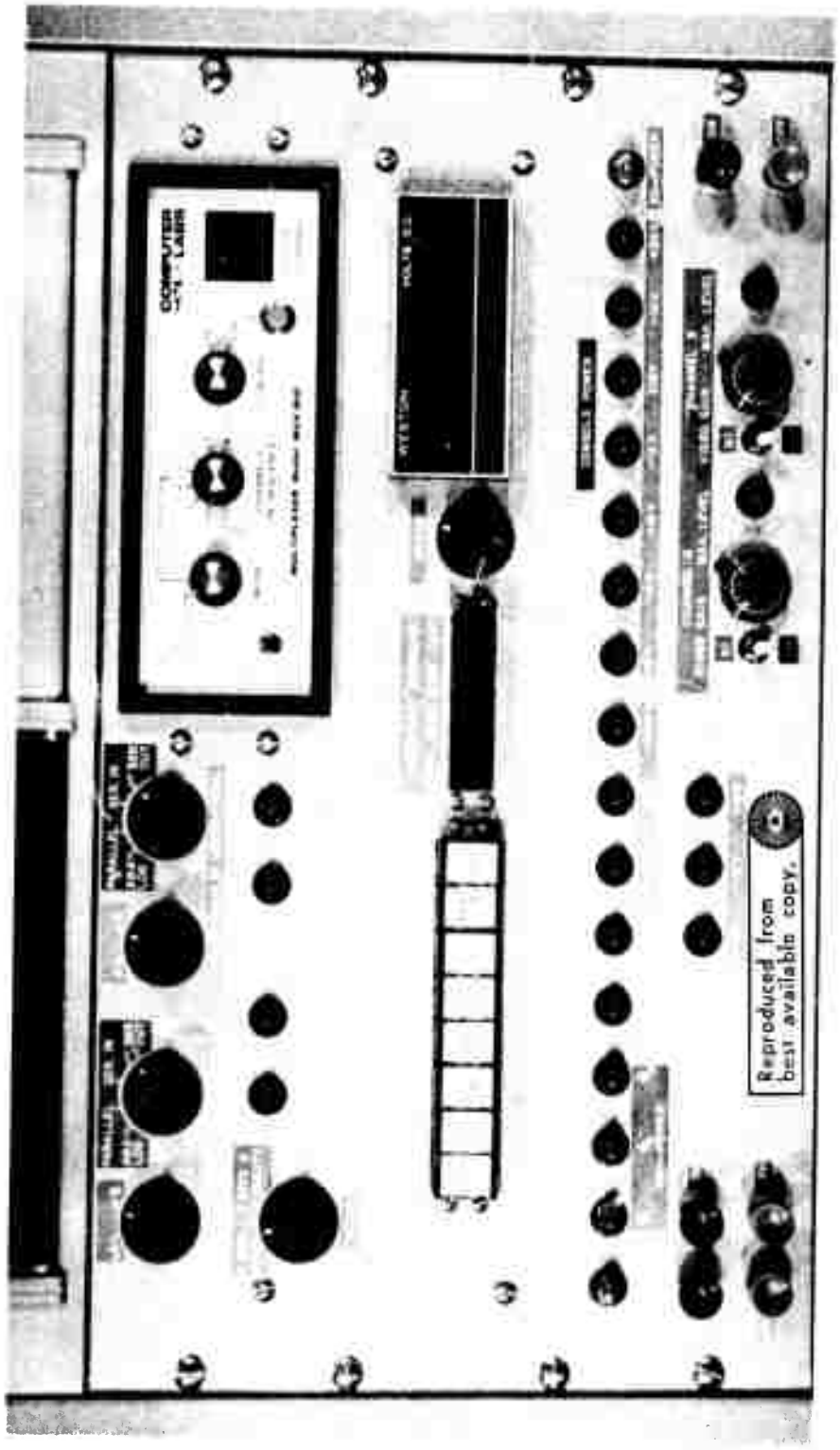


Fig. 11. Console control unit, system operating controls.

TABLE II
SYSTEM OPERATING CONTROLS AND INDICATORS
CONSOLE CONTROL UNIT

Control or Indicator	Function
Console Main Power ON/OFF	Controls Primary Power to all Console Components, Including the 28 v dc supply used for scanner stepping motors and power control relays
Scanner Main Power 60 ∿ON/OFF	Controls Primary Power to all Scanner components except for the scanner motor.
400 ∿ON/OFF	Scanner motor control.
	These controls are operational only when console main power is ON.
Console Power Indicators	These indicator lamps, when illuminated, indicate proper operation of the corresponding console power supplies.
Scanner Power Indicators	These indicator lamps, when illuminated, indicate proper operation of the corresponding scanner power supplies.
Stepping motor selectors:	Selects a particular stepping motor for positioning optical components within the scanner package. Illuminated push button indicates which motor has been selected.
TRANS. A	Controls translation of the A channel image separator corner reflector.
HORIZ. A	Controls A channel horizontal image positioning
VERT. A	Controls A channel vertical image positioning
TRANS. B	Controls translation of the B channel image separator corner reflector
HORIZ. B	Controls B channel horizontal image positioning
VERT. B.	Controls B channel vertical image positioning
MAGNIFICATION	Controls motion of the translation stage used to position optical components for obtaining magnifications of 1:1, 2:1, or 4:1
TARGET	Inserts or removes cross-hair alignment targets at the primary focus in both the A and B channel optical paths

TABLE II
(Continued)

Control or Indicator	Function
Stepping Motor Controls:	
INCREASE FAST	Produces clockwise rotation of selected stepping motor and an increase in stepping motor position indicator readout at a speed de-determined by the stepping motor SPEED control
DECREASE FAST	As above except counterclockwise rotation and a decrease in position indicator readout are produced.
INCREASE SLOW & DECREASE SLOW	As above except stepping motor speed is approximately 1 pulse per second, independent of speed control setting
SPEED	Controls speed of stepping motors when FAST controls above are in use
Stepping Motor Position Indicator (Digital Voltmeter)	Provides a numerical readout proportional to the current position of the selected stepping motor within its range of travel and hence provides a means for resetting a stepping motor to any desired pre-determined position. An over voltage or undervoltage indication signifies the motor has reached the end of its travel in that particular direction
Channel A & Channel B VIDEO GAIN	Controls gain of the corresponding A or B channel video amplifier located in the scanner control unit
HI-LO	Selects high or low gain for the video filter amplifier located in the scanner logic unit (console card cage)
MAX. LEVEL	This indicator, when lighted, indicates that a full scale reading has been obtained from the A/D converter for the corresponding A or B channel video signal

TABLE II
(Continued)

Control or Indicator	Function
Display Unit 1 or 2:	
CHANNEL SELECTOR	Selects A channel or B channel video for viewing on the corresponding display unit. Also connects mode and parity indicators (see below) to the selected channel.
VIDEO SELECTOR	Permits viewing of video data at various points in the system: ANALOG - analog video prior to multiplexing PARALLEL - digital video following A/D conversion and demultiplexing SERIAL IN - serial data stream (decoded) prior to recording SERIAL OUT - serial data stream (decoded) reproduced from magnetic tape
PARITY MODE	When illuminated, indicates that parity mode has been selected (see below) during recording (SERIAL IN), or that a tape is being reproduced (SERIAL OUT) which was previously recorded using the parity check mode.
PARITY ERRORS	This indicator flashes each time a parity error is detected
MODE SELECTOR	Selects recording mode for both channels. Either 8 data bits per word, or seven bits plus parity may be recorded.

TABLE III
AUXILLIARY CONTROLS AND INDICATORS

Unit	Control or Indicator	Normal Setting	Function
X-Y Display (HP 1330 A)	FOCUS	Focused Spot	Focus
	INTENSITY	≈2/3 cw	Image Intensity Level
	POSITION VERTICAL	Centered	Vertical Centering
	POSITION HORIZONTAL	Centered	Horizontal Centering
	LINE ON	ON	Main Power
Multiplexer (CL MUX-810)	ON-OFF	ON	Main Power
	RANDOM ACCESS/SEQUENTIAL	RANDOM ACCESS	Addressing Mode Selector
	CHANNELS IN SEQUENCE	2	Selects number of input channels
	CONTROL	EXT	Selects external channel address input
	Push Button (Red)	Not Used	Can be used to select a channel manually in sequential mode & man. control positions
	ACTIVE CHANNEL	1 & 2 (scanner on) 1 or 2 (scanner off)	Indicates present channel selected
A/D converter (CL HS-802)	Output indicators	Blinking (scanner on)	Indicates current output of A/D converter
	1/0, Binary bits 1-8	Random (scanner off) (see TEST below)	Bit 1 = MSB, Bit 8 = LSB
	TEST	Center (off)	A/D converter operational check - see Table IV
	MODE	COMMAND	Holds current output until encode command initiates a new conversion cycle
	CODE	BINARY	Selects binary rather than gray code output
	POWER	ON	Main power

TABLE III
(Continued)

Unit	Control or Indicator	Normal Setting	Function
Logic Power Supply (LPS-1)	REMOTE-OFF-ON	Remote	Permits main power control via the logic control unit push buttons
	MAIN POWER	In	Main Power circuit breaker - push to reset
	Power ON	ON	Primary Power Indicator
	Fuse Indicators	Off	Lighted Indicator signifies blown fuse

TABLE IV

A/D CONVERTER TEST CODES

Code	Test	Correct Readout
Binary	1	11001100 or 11001011 or 11001101
	2	01100110 or 01100101 or 01100111
Gray	1	10101010 or 10101110 or 10101011
	2	01010101 or 01010100 or 01010111

The recorder control panel located in the control console duplicates many of the functions found on the front panel of the recorder and permits operation of the recorder from the console once a tape has been mounted, main power and transport power have been turned on, and tape speed has been selected. Lighted push buttons for RECORD, STOP, REWIND, FORWARD, and REPRODUCE are provided on this panel as are indicaters for READY, RECORD SPEED (120 ips tape speed selected) and RECORD SPEED ERROR (tape speed other than 120 ips selected).

The scanner control unit, CU-2 (see Fig. 12) contains a duplicate set of controls and indicators for scanner power and stepping motor positioning and readout which may be used interchangeably with those on the console control unit. The scanner control unit also contains a small display scope and associated controls for visual observation of the analog infrared images received by the scanner. In addition to the normal oscilloscope controls, a CHANNEL SELECTOR switch and VIDEO GAIN control (completely independent from those which control the console indicators and recording system) are provided.

2. Operating Procedure

a. System turn on procedure

With system installed and interconnected as in Section A, above:

1. Set all auxiliary controls to the normal settings given in Table III.

2. Press console main power ON button located on control unit CU-1.
   a. MAIN POWER pilot lamps on logic power supply and control unit should light.
   b. CONSOLE POWER supply indicators on control unit should light.
   c. 24 V. INDICATOR on scanner control unit should light.
   d. POWER INDICATORS and/or NUMERICAL READOUTS on console control unit digital voltmeter, multiplexer, A/D converter, and console display units should light.

3. Press scanner power 60∿ ON button located on console control unit CU-1 or scanner control unit CU-2.
   a. Scanner MAIN POWER pilot lamps on console and scanner control units should light.
   b. Scanner power supply indicators on console and scanner control units should light.
   c. Digital voltmeter on scanner control unit should be illuminated.
   d. A dot should be visible on scanner control unit display scope if scope intensity control is advanced. (Note: Reset intensity control if necessary so that screen will not be burned.)

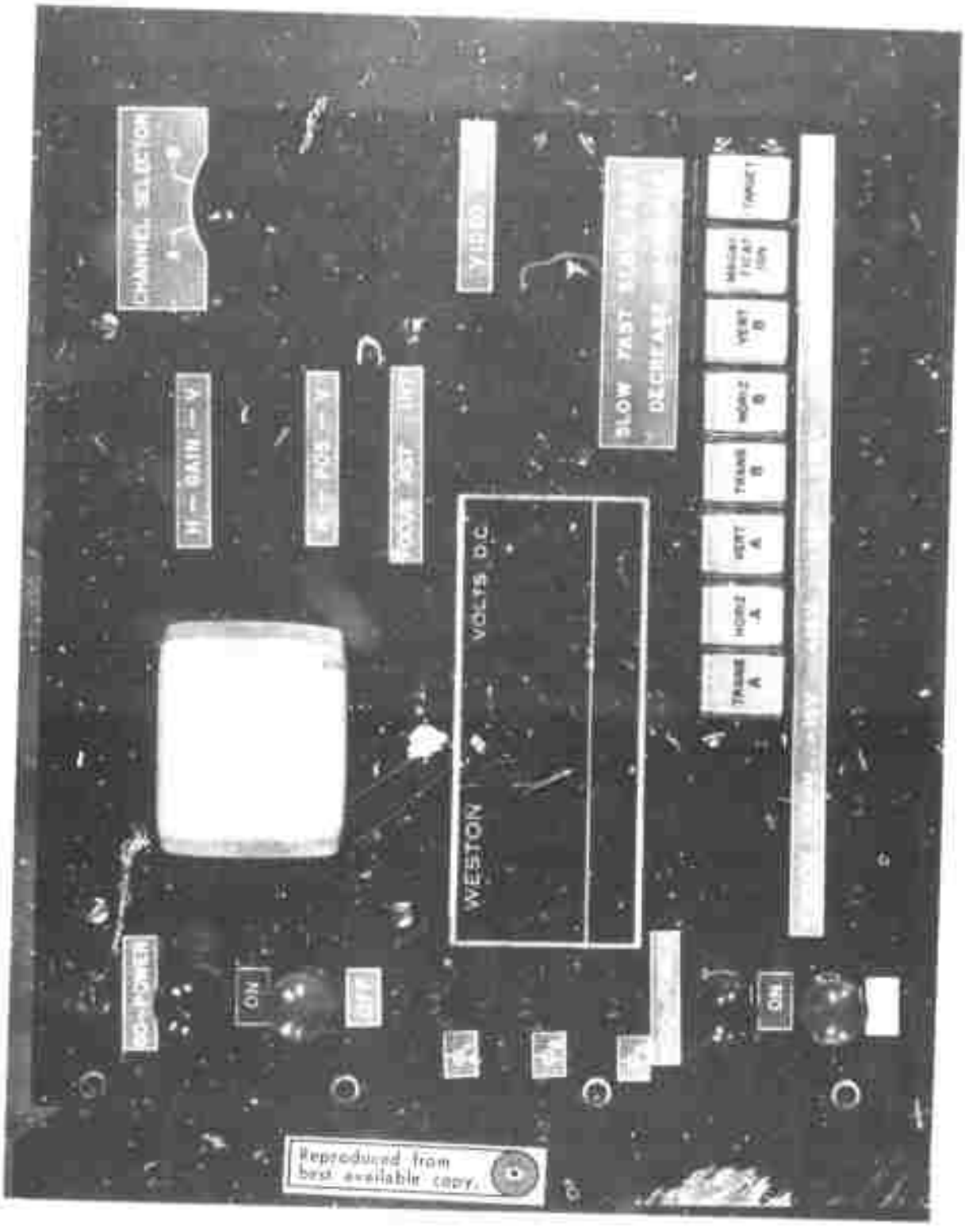


Fig. 12. Scanner control unit, operating controls and display unit.

4. Press scanner power 400∿ ON button located on console control unit CU-1 or scanner control unit CU-2
   a. 400∿ POWER indicators on console and scanner control units should light
   b. Scanner motor should start.
   c. When motor is up to speed, a 40 x 40 raster (dot pattern) should appear on the scanner control unit display scope. (Readjust INTENSITY, FOCUS, POSITIONING, and GAIN controls for best pattern, if required.)
   d. Similar rasters should appear on the console display indicators when the corresponding VIDEO SELECTOR switches are in the ANALOG, PARALLEL, or SERIAL IN positions. (Adjust indicator controls for best pattern, if required.)
   e. With VIDEO SELECTOR switches in the SERIAL IN position, and the MODE SELECTOR in the 7 BITS + PARITY position, the corresponding MODE indicator lights should light. PARITY ERROR indicators should be out indicating that no errors are present. (Error indicators may be checked if desired by turning off scanner motor briefly, allowing the disc speed to drop below required limits. Errors should then be present in the signal supplied to the decoder, causing the ERROR indicators, and possibly also the MODE indicators, to blink.)

5. Turn on tape recorder by pressing the POWER button on the recorder front panel. (NOTE: circuit breaker inside the tape recorder control drawer must be ON.)

6. Mount a tape on the transport as described in the operators manual furnished with the tape recorder.[8] NOTE: A tape to be used for recording must be thoroughly degaussed prior to mounting on the tape transport; otherwise the error rate of the recorded data will be significantly increased.

7. Set the TAPE SPEED selector on the recorder front panel to 120.

8. Press the TRANSPORT button on the recorder front panel.
   a. The POWER, TRANSPORT, READY, and STOP indicators on the recorder front panel should be illuminated.
   b. The RECORD SPEED, READY, and STOP indicators on the recorder control panel in the console should be illuminated.

The recorder can now be operated from the front panel controls or from the control console, as desired.

To obtain minimum error rate without realignment of the Miller code electronics, the recorder should be turned on (steps 6 through 8 above) at least one hour prior to use.

b. Scanning and displaying an infrared image

With system operating as described above

1. Apply high pressure clean, dry nitrogen to the detectors via the connector on the scanner mounting plate. A suitable pressure regulator should be used so that pressures of 1000-1500 psi can be obtained. Detector cooling requires approximately 15 minutes at 1500 psi. After operating temperature has been reached the pressure may be reduced if desired to conserve nitrogen. Pressures down to approximately 1000 psi usually provide satisfactory operation. If cooling becomes erratic, increase pressure.

2. A 10.6 micron image containing on the order of 2 milliwatts of average power may now be applied to the scanner via the optical system. With proper adjustment of the video gain and image positioning (stepping motor) controls, the image should be displayed on the scanner control unit display scope and console display units.

3. For test and alignment purposes, cross hair targets are provided which may be lowered into the optical path near the primary focal plane. To lower these targets, press the TARGET selector button on either the scanner or console control unit and then press the stepping motor DECREASE FAST button until the stepping motor position indicator (digital voltmeter) gives an underrange indication signifying that the targets are fully lowered. The stepping motor is stopped automatically in this position and the DECREASE FAST button has no further effect. (Targets may be raised when desired by pressing the INCREASE FAST button with TARGET selector button depressed as above. The stepping motor automatically stops with targets in the fully raised position and with the stepping motor position indicator giving an overrange indication.)

   A flood beam such as a diffuse beam from a 10.6 micron laser (total average incident power $\approx$2 mw) may now be applied (by imaging a diffuse field via the primary optics or by directly flooding the scanner input aperture), thus casting shadows of the target cross hairs which are imaged by the scanning detector. These target images are quite useful for setting the translation stage for a given magnification and for centering an image to be viewed in the optical field of view of the detector.

4. Image Positioning, selection of magnifications of 1:1, 2:1, or 4:1, and field separation for the two channels (see Chap. II, Section A) may be accomplished as desired by means of the stepping motor controls on either the console or scanner control unit. It is suggested, following initial installation, that frequently used positions of the various stepping motors

(i.e., magnifications, centered-field image positions, etc.) be calibrated using the cross hair targets and stepping motor position indicator so that indicator readout can then be used to reset the stepping motors to these positions.

5. Video gain and display scope controls on the scanner control unit should be adjusted to obtain the best visual display. Either the channel A or channel B image may be selected via the channel selector switch.

6. Channel A and Channel B video gain for the control console displays, and for recording, should each be adjusted as follows:

   a. Increase gain of one channel using the VIDEO GAIN control and HI-LO switch as required until the corresponding MAX LEVEL indicator lights.
   b. Decrease the gain slowly until the MAX LEVEL indicator is just extinguished, or flashes occasionally.
   c. Repeat for the other channel. (If only one channel is to be used, set gain of the unused channel to minimum.)

Note that if the signal level for one or both channels is set too high, cross coupling between channels will occur due to overloading at the multiplexer and A/D converter. Hence, if difficulty is obtained in adjustment of the first channel, as above, decrease gain setting of the other channel.

For maximum signal to noise ratio, the HI-LO switch should be in the LO position whenever signal level permits. This insures that maximum video amplification takes place in the scanner, prior to any line induced noise, rather than in the scanner logic unit where any noise picked up by the lines would also be amplified.

7. Adjust the intensity, focus, and positioning controls on the display indicators, if required for best visual presentation.

Note that the orientation of the images appearing on the display indicators may differ from that of the image received by the primary optics (see Section 3 below).

c. Recording

With the system in operation, the recorder on, and an image being received as described above, and assuming that a previously degaussed tape has been mounted (see paragraph a-6) the image data being received may be recorded.

1. Check video gain and readjust if necessary (paragraph b-6).

2. Make sure recording speed (120 ips) has been selected (paragraph a-7) and that the tape recorder capstan is up to speed as indicated by a stationary pattern on the innermost section of the stroboscope disc attached to the capstan. (NOTE: 60 cycle illumination such as ordinary room lighting-not sunlight - must be used to observe the stroboscope pattern.)

WARNING: Do not proceed to Step 3 until capstan has reached operating speed, otherwise the tape may be damaged.

3. Simultaneously press both RECORD buttons on either the recorder front panel or console mounted recorder control panel. After several seconds delay required to get the tape up to speed and lower the record and reproduce heads the RECORD indicators (push buttons) should be illuminated indicating that recording is in progress.

4. After an additional delay of approximately 10 seconds (during which time an 0101 code is being recorded for clock synchronization upon subsequent playback) the recorded image, read back from the tape immediately after recording, may be viewed on a console display unit by setting the corresponding VIDEO SELECTOR to the SERIAL OUT position. Since two identical display units are provided, images from both channels may be viewed simultaneously, if desired.

5. If the MODE SELECTOR is set to record the 7 bits + parity mode and the display unit VIDEO SELECTOR is set to the SERIAL OUT position, as above, the corresponding PARITY MODE indicator should be lit and any errors detected during playback of the recorded data will cause the PARITY ERROR indicator to blink.

An average error rate of one every several seconds is normal for this system (see last paragraph of Chapter II). In practice, errors usually occur in bursts with longer periods of error-free data between. Abnormally high error rates usually indicate one or more of the following conditions which should be corrected:

a. recorder not adequately warmed up prior to use (or room temperature environment not maintained)
b. tape not thoroughly degaussed prior to recording
c. dirty recording or playback heads
d. magnetized recording or playback heads
e. dirty or defective tape, or tape of incorrect and inadequate quality
f. playback head azimuth requires adjustment
g. Miller code system requires alignment
h. record level or bias controls require adjustment.

Alignment procedures are given in Appendix IV. Since these should rarely be required, all other possibilities should first be eliminated.

d. Playback of a prerecorded tape

To reproduce a previously recorded tape for viewing, the console and recorder should be turned on and the tape should be mounted as previously described in paragraph a. For minimum error rate the recorder should be allowed to warm up prior to use, as mentioned previously. The scanner power need not be turned on.

1. Select the desired tape playback speed via the TAPE SPEED selector on the recorder front panel.

   a. Either 120 ips or 15 ips may be selected.
   b. The 30 ips or 60 ips positions may not be used since the Miller code electronics permits simultaneous installation of only two filter sets, presently chosen to be 120 ips (required for recording) and 15 ips.

2. When recorder capstan has reached operating speed (see WARNING, paragraph c-2 above) as indicated by a stationary stroboscope pattern (outer segment for 15 ips, inner segment for 120 ips) press REPRODUCE button on either the recorder front panel or console mounted recorder control panel.

3. The recorded images may now be viewed on the display units provided the corresponding VIDEO SELECTORS are set to the SERIAL OUT positions.

4. If the tape has been recorded using the 7 bits + parity mode, the PARITY MODE indicators should be illuminated and the information concerning errors given previously in paragraph c-5 is applicable.

5. Recorder speed may be changed (see 1. above) during reproduction without risk of tape damage (the image will lose sync., however during speed changes) provided that the recorder is kept in the REPRODUCE mode. If the recorder is in the STOP mode, however, and a speed change is made, the capstan must be allowed to reach the new operating speed before REPRODUCE is again iniated; otherwise tape damage will likely occur.

e. System turn off procedure

1. Turn off nitrogen supply to detectors

2. Turn off recorder by pressing TRANSPORT and/or POWER buttons on recorder front panel.

3. Turn off scanner power by pressing 60∿ and 400∿ OFF buttons on scanner control unit or on control console. (This step may optionally be omitted since step 4 below will automatically turn off scanner power.)

4. Turn off console power by pressing console main power OFF button on console control unit.

3. Image Orientation and Scanning Sequence

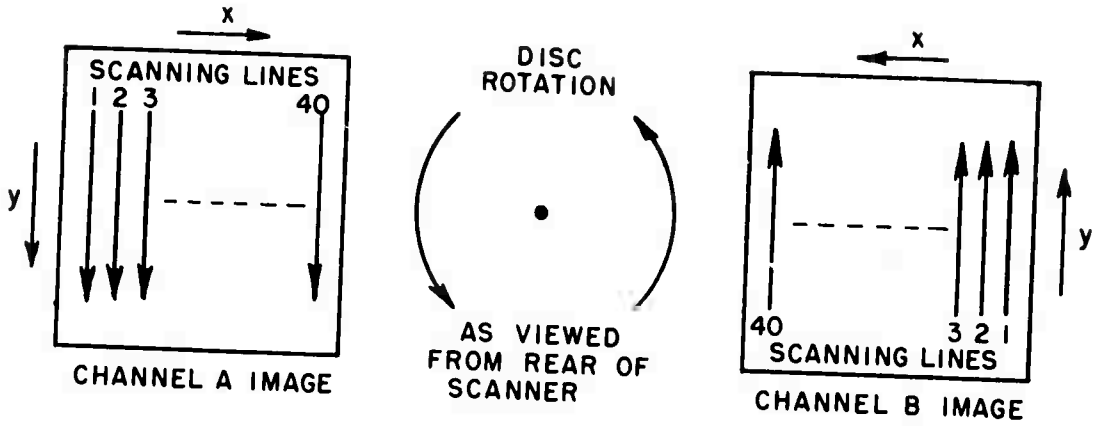
Because of the method of scanning (see Chapter II, Section A) as well as the primary optics used the images appearing on the display

indicators may be reversed (left-to-right) or inverted (top-to-bottom) with respect to the incident image. For most applications knowledge of this orientation will be required.

Images incident at the scanner unit input aperture, for both A channel and B channel, are transmitted to the scanning disc by the magnifying and positioning optics without reversal or inversion, hence image orientation at the scanning disc is identical to that at the input aperture. However, since the A channel and B channel images are simultaneously scanned by opposite edges of a single scanning disc, the scanning sequence for channel A differs from that for channel B as shown in Fig. 13. Note that the x-y coordinate vectors shown for each image in this figure are determined by the order in which successive image elements are scanned. These coordinate vectors are displayed with conventional orientation on all system display indicators as shown in Fig. 14. Consequently, A channel images are inverted (top-to-bottom) and B channel images are reversed (left-to-right) on all display indicators, as compared to the images incident at the detector input. Depending upon the primary optics used in a particular installation, an additional reversal and/or inversion may be present prior to the scanning detector input, hence effects of the primary optics must also be considered in determining final image orientation.

If the second display indicator has been installed in the console (see paragraph A-1, above), and if one indicator is always used to display A channel images while the other is always used to display B channel images, then properly oriented image displays for both channels may be obtained, if desired, by appropriate reversals of polarity of the x and/or y axis inputs to the display indicators as described in the manual supplied with the indicator unit.[7] Since the scanner control unit contains only one indicator, and since no convenient means for reversing the input polarities to this unit is provided, image orientation for the scanner display will remain as previously described.

The order in which image information is written on magnetic tape is the same as the scanning sequence given in Fig. 13. Each image line consists of 40 equally spaced words (i.e., 40 distinct dots on the indicator display) which are sampled, recorded, and reproduced, in numerical order, in the direction indicated by the arrows representing the scanning lines. Successive lines are not generated, recorded, and reproduced in numerical order, however, but are interlaced 2 to 1 according to the sequence given in Fig. 13.



EACH VERTICAL SCANNING LINE CONTAINS 40 WORDS SCANNED IN SEQUENCE (1, 2,--- 40) AS INDICATED BY DIRECTION OF ARROW

HORIZONTAL SCAN IS INTERLACED WITH LINE SEQUENCE (1, 3, 5,---- 39, 40, 38, 36,---- 4, 2)

Fig. 13. Scanning sequence.

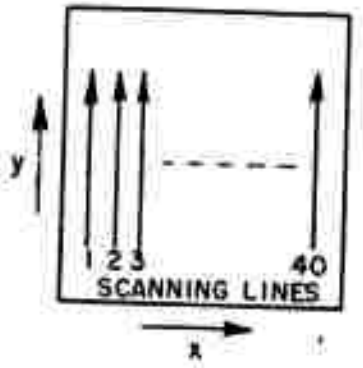


Fig. 14. Display sequence.

IV. THEORY OF OPERATION

This chapter contains details of the individual units, circuit groups, and logic cards comprising the 2-channel infrared scanner system. Frequent reference is made to the logic, schematic, and timing diagrams of Appendix I throughout the following sections.

Logic wiring diagrams are first presented which essentially parallel the system block diagram given earlier in Fig. 2, but are considerably more detailed. Wiring diagrams for the major system components are then given followed by logic and timing diagrams for the individual circuit cards and subassemblies.

With the exception of the linear video amplifiers, video switching, line drivers and receivers, and stepping motor limit controls, all logic components are standard TTL integrated circuits. For additional information on the individual IC's the manufacturers literature[10-13] should be consulted.

A. Logic Wiring Diagrams

Logic wiring diagrams for the telescope-mounted package (scanner and scanner control unit CU-2) and for the system control package (console units and magnetic tape recorder) are given in Figs. 20 and 21, respectively, of Appendix I. Functional circuit groups and/or circuit boards are shown on these diagrams as appropriately labeled rectangles with interconnections shown and directions of signal flow indicated. Card slots occupied by all printed circuit cards are given by the circled numbers within the rectangles, and card cage pin numbers are given for all interconnections to each card. Interconnections labeled "Front Edge Connector" are made via the special edge connector bolted to the front edge of a circuit card, while all other interconnections are made via the standard card cage (rear edge) connectors. Where signal paths are completed via intervening connectors, the corresponding connector numbers are given.

In addition to providing detailed information on the various circuit groups and signal paths, these diagrams show all card cage connections, and hence serve as card cage wiring diagrams. All circuit cards for the telescope-mounted package are located in the scanner control unit CU-2, while all cards for the control package are located in the console mounted scanner logic unit SLU-1.

Certain components such as channel selectors and video gain controls included in these diagrams for functional completeness may be found in more detail in schematics for the specific units containing them (see Section B. below).

The general theory of operation for the complete system, for which these diagrams illustrate all logic components, has been presented previously in Chapter II. Additional details of individual components are given in subsequent paragraphs.

B. Major System Components

1. Scanner

The scanner unit contains magnifying and positioning optics, stepping motors and control relays, scanning disc and motor, video detectors with Perry Preamps, and the sync projectors and detectors with their power supplies and voltage divider network.

A photograph of the scanner with cover removed is given in Fig. 15 while the scanner with disc, motor, and sync assembly removed in order to show the optical components and stepping motor assemblies is shown in Fig. 16. The disc, motor, and sync assembly, as viewed from the front, is given in Fig. 17. Wiring diagrams for the scanner and for one of the eight stepping motor assemblies are given in Figs. 22 and 23, respectively, of Appendix I. All stepping motor assemblies are electrically identical although gearing and mounting details differ for the various units as shown by the photographs.

The various scanner components are identified by number in the photographs and are listed in Table V.

Video and sync signal outputs are provided via BNC connectors while all stepping motor control and power connections are via connector P17 to the scanner control unit CU-2 which is attached to the scanner mounting plate.

2. Scanner Control Unit

The scanner control unit CU-2 which is bolted to the front plate of the scanner package contains scanner power controls and indicators, stepping motor controls and position indicator, and a small visual display indicator with associated CRT controls,[14] video gain control, and channel selector switch. Functions of these controls and indicators are described in Chapter III-B and in Table II while a front panel photograph is given in Fig. 12. This unit also contains a card cage for the telescope-mounted logic circuits (see Section A above and Fig. 20), power supplies,[15,16] and a cooling fan.

Test points are provided near the edge of the card cage (see Fig. 18) from which various sync. signals are available for testing and alignment. All electrical connections to the telescope-mounted package are made via the scanner control unit connector panel, Figs. 10 and 18, which also contain primary power fuses and a circuit breaker.

A wiring diagram for the scanner control unit is given in Fig. 24 of Appendix I.

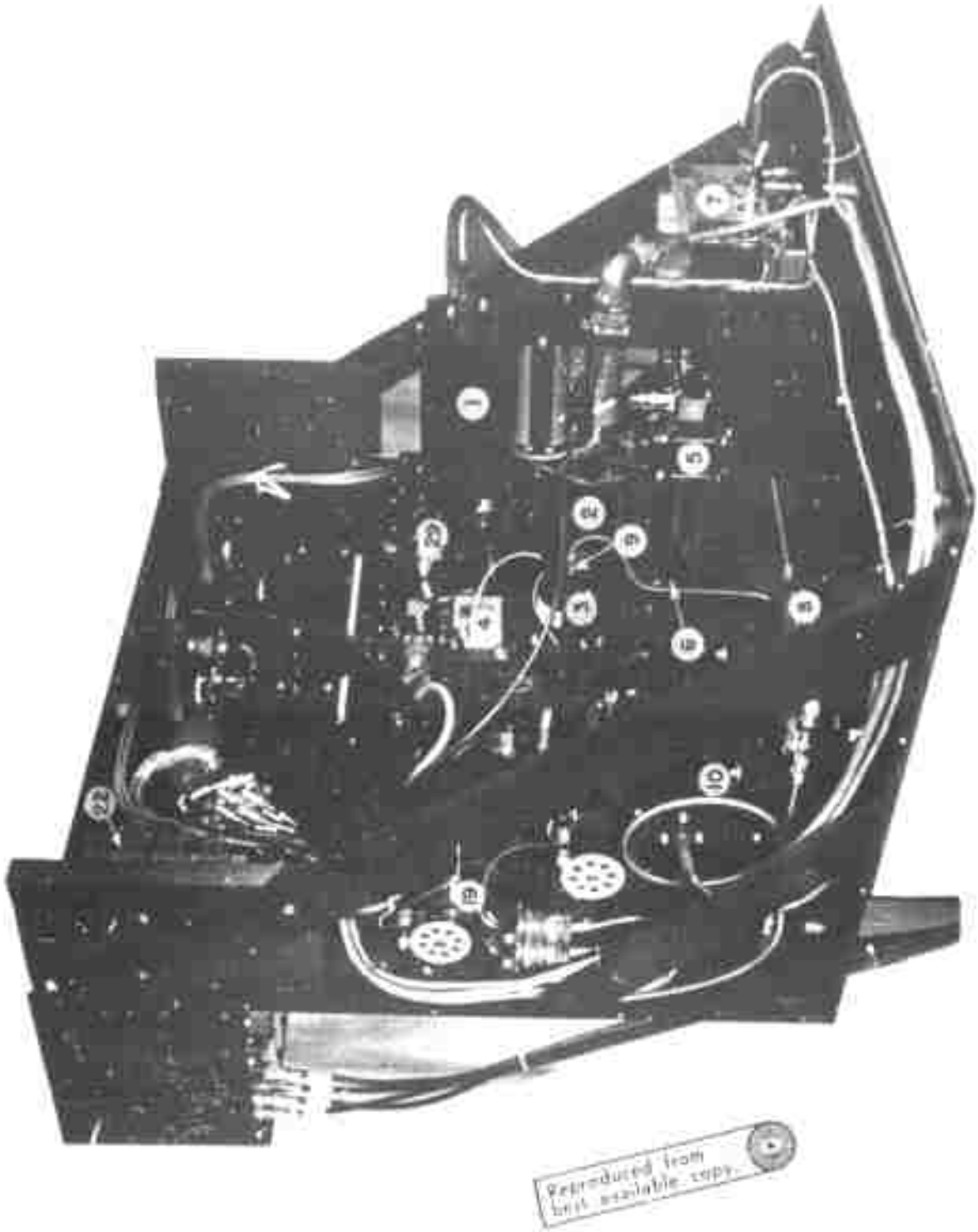


Fig. 15. Rear view of scanner with cover removed.

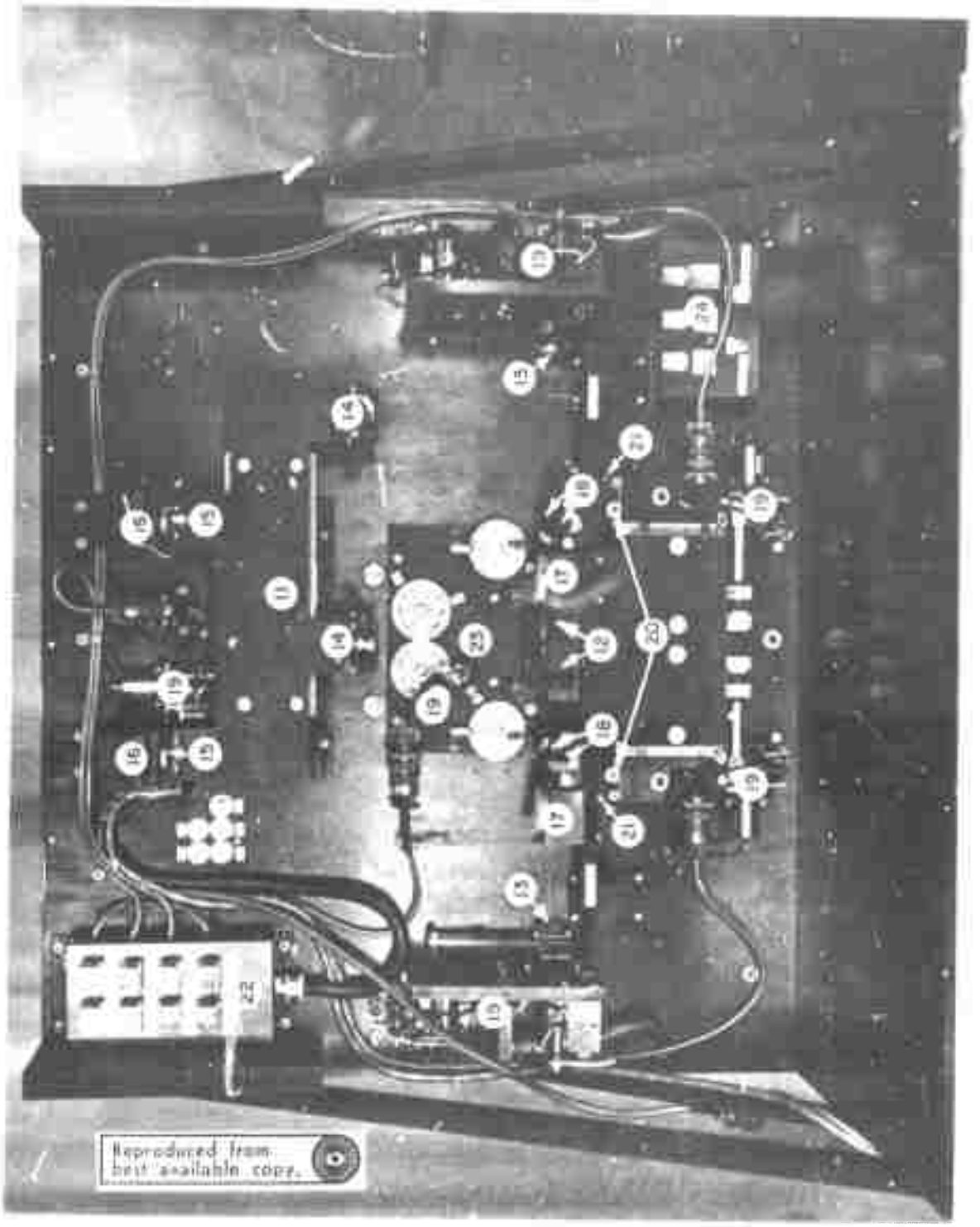


Fig. 16. Scanner optical system and stepping motor servos.

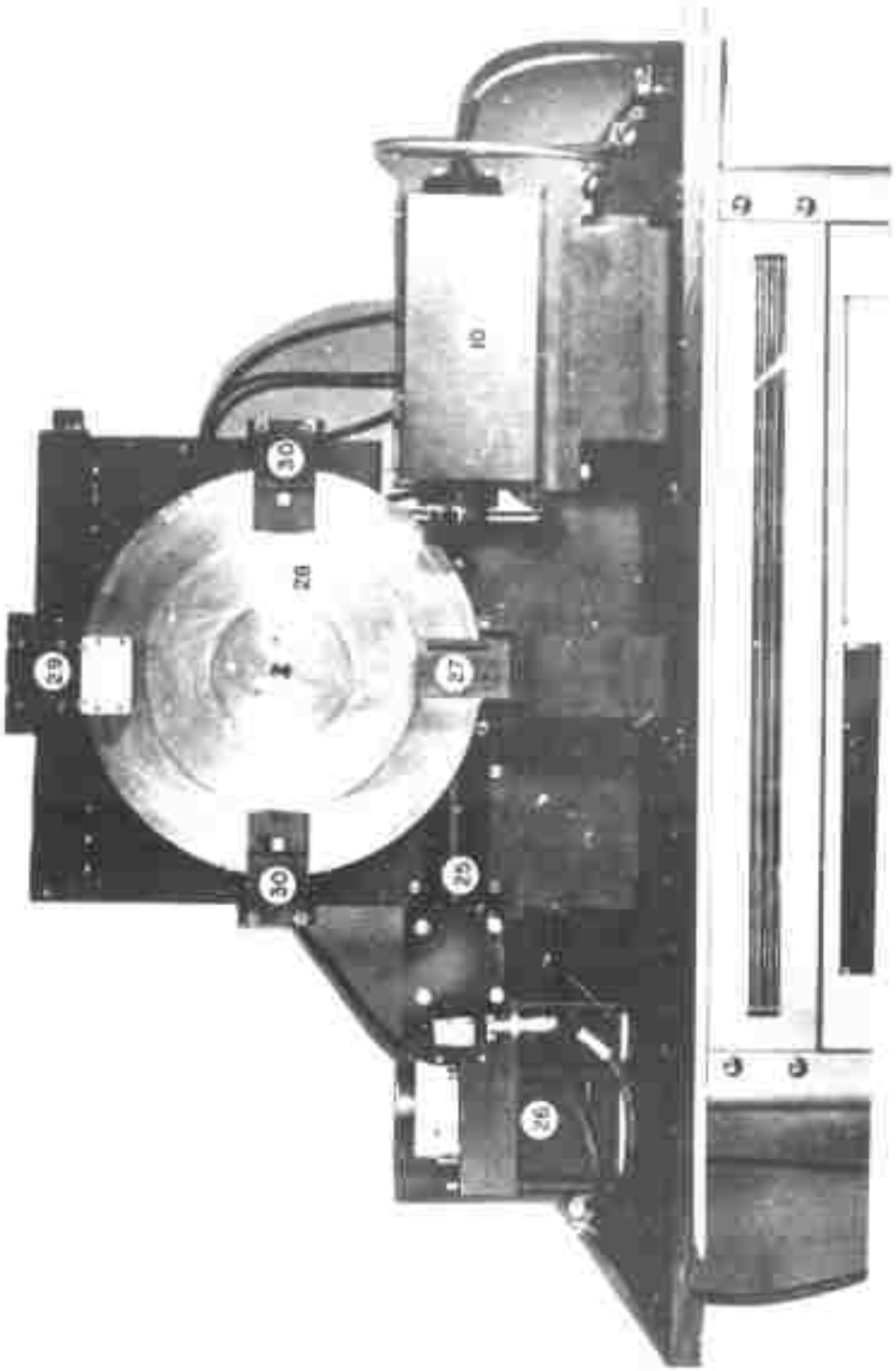


Fig. 17. Scanning disc and sync assemblies.

TABLE V
SCANNER COMPONENT IDENTIFICATION

Number	Figure	Component
1	15	Line, frame, and disc sync projector
2	15	Scanner motor
3	15	IR detector mount (Channel A)
4	15	Perry preamp (Channel A)
5	15	Odd word sync detector
6	15	Word sync splitting mirror
7	15	+5.5 v. power supply PS1
8	15	Nitrogen filters
9	15	Cryostat (Channel A)
10	15,17	Word sync projector
11	16	Magnification translation stage
12	16	Image separator corner reflectors
13	16	1st parabolic mirror (200 mm. f.l.)
14	16	2nd parabolic mirror, 1:1 magnification (200 mm. f.l.)
15	16	2nd parabolic mirror, 2:1 magnification (400 mm f.l.)
16	16	Beam folding flat for 4:1 magnification
17	16	2nd parabolic mirror, 4:1 magnification (800 mm f.l.)
18	16	Optical flats
19	15,16	Stepping motor servo (typical)
20	16	Image separator rotation adjust micrometer
21	16	Image separator tilt adjustment screw
22	15,16	Stepping motor relay panel
23	16	Target assembly
24	16	Sync detector high voltage divider
25	17	Even word sync detector
26	17	-1250 volt power supply PS2
27	17	Word sync projection mirror
28	17	Scanning disc
29	15,17	Line, frame, and disc sync detector
30	17	Image framing masks

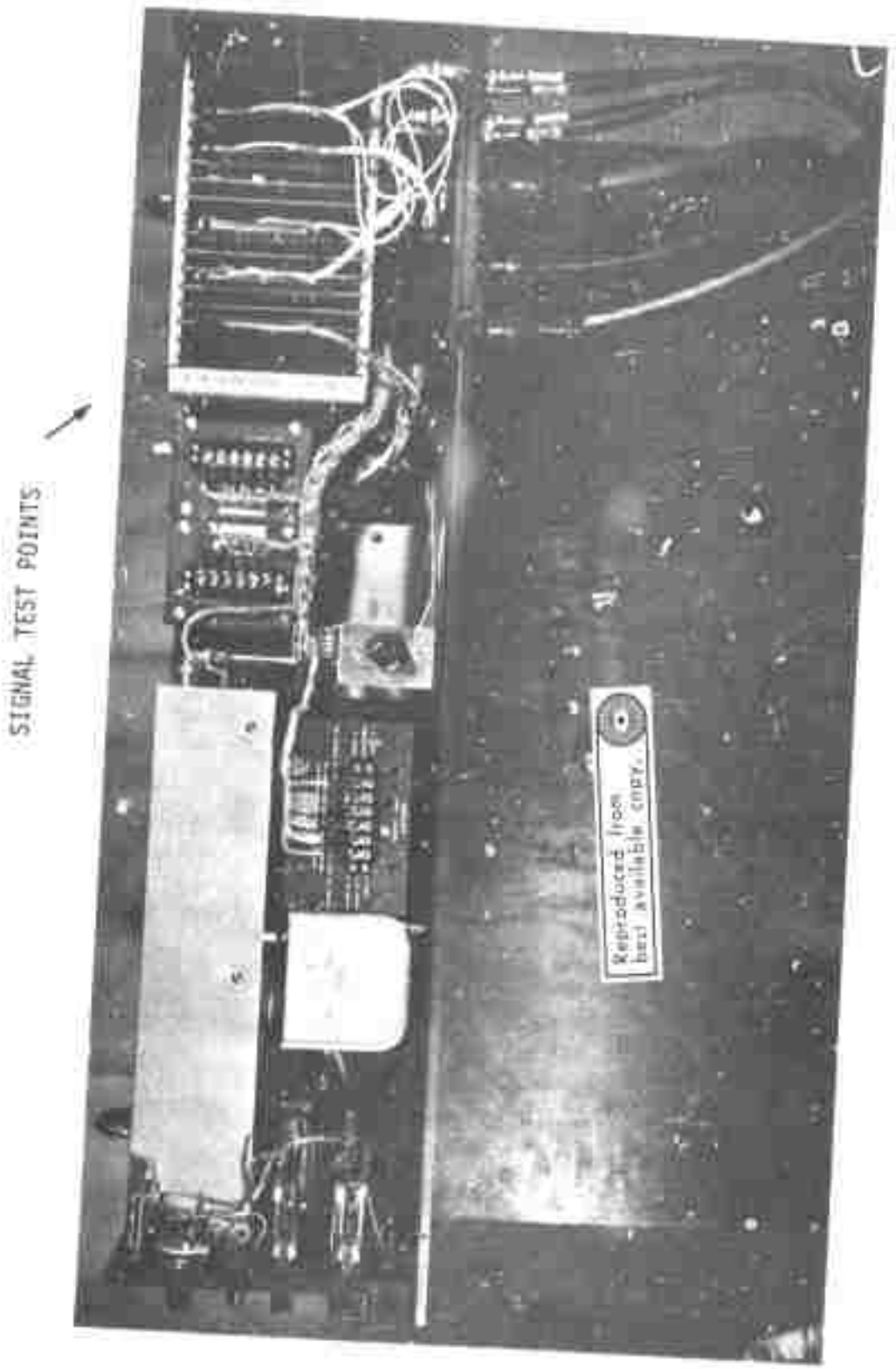


Fig. 18. Scanner control unit with cover removed.

3. Console Control Unit

The console control unit CU-1 contains all of the main operating controls for the scanner system as previously described in Chapter III-B and Table II. A front panel photograph showing the various controls and indicators is given in Fig. 11 and a wiring diagram is given in Fig. 25, Appendix I.

In addition to the controls and indicators, this unit contains the stepping motor controller, pulse source and limit control, and timing relays, RY1 and RY2 of Fig. 25, to pulse the stepping motor selector switch release solenoid for either the console control unit or scanner control unit when a button on the opposite control unit is pressed. Power is applied to one of these relays when a button on the corresponding console is pressed. The relay pulls in, energizing the release solenoid for the other console push buttons, for the time interval required to charge timing capacitor C1 or C2. The parallel resistors R1 and R2 provide discharge paths for the capacitors after power is removed, but limit current through the relay to a value too low to keep the relay pulled in with power applied.

The stepping motor pulse source provides positive pulses of 10 volts magnitude or greater to drive the stepping motor controller. A pulse rate of 1 pulse per second (SLOW) or a variable rate up to several hundred pulses per second (FAST) determined by the setting of the SPEED CONTROL can be applied to the stepping motor controller via the INCREASE or DECREASE, FAST or SLOW, buttons on the scanner or console control unit. The stepping motor controller provides output pulses required to drive a stepping motor in the desired direction when the appropriate controller input is pulsed. These pulses are applied to the stepping motor selected by one of the selector buttons on the scanner or console control unit via the corresponding relay in the scanner (see Fig. 16). This relay also connects the selected stepping motor position potentiometer to the digital voltmeter position indicators located on the scanner and console control units. The stepping motors, pulse source, and controller are standard commercial items (see Figs. 23 and 25), and the manufacturers literature should be consulted if further information is required on these components.[17]

The stepping motor limit control operates in conjunction with the digital voltmeter position indicator to limit stepping motor travel in each direction to the proper range, thus preventing damage to the gearing, position pots., or other components. The digital voltmeters, located on both scanner and console control units for position indication via the voltage supplied by the selected stepping motor position potentiometer, are commercial components (see Figs. 24 and 25) and the manufacturers literature[18] should be consulted for additional information. These meters have been modified, however, as follows, for use in this system:

(1) The voltmeters which had a 0-10 volt range were converted to read full scale with only 5 volts applied by shorting out

one of the two equal multiplier resistors (R105 and R106 on the schematic furnished by the manufacturer[18]).

(2) The response time of the meters have been decreased by replacing the 1.0 microfarad input filter capacitors C101 and C102 by 0.1 microfarad capacitors.

(3) On the meter used in the console control unit only, outputs for digital readout, over-range, under-range, and print command have been brought out to the pc edge connector. The direct (zeroing) input originally connected to pin 1 has been removed and this terminal is used for one of the above outputs (see Table VI).

TABLE VI
DIGITAL VOLTMETER CONNECTIONS

Pin	DVM FUNCTION	
	Console Unit	Scanner Unit
1	Under-Range	Direct Input (Gnd. for zero set)
2	Print Command	N.C.
3	Units "1" Output	N.C.
4	Units "4" Output	N.C.
5	Tens "1" Output	N.C.
6	Tens "4" Output	N.C.
7	Hundreds "1" Output	N.C.
8	Hundreds "8" Output	N.C.
9	Over-Range	N.C.
10	Power Gnd.	Power Gnd.
A	Voltage Input (-)	Voltage Input (-)
B	Voltage Input (+)	Voltage Input (+)
C	Units "2" Output	N.C.
D	Units "8" Output	N.C.
E	Tens "2" Output	N.C.
F	Tens "8" Output	N.C.
H	Hundreds "2" output	N.C.
J	Hundreds "4" Output	N.C.
K	115 v 60 Hz Power (N)	115 v 60 Hz Power (N)
L	115 v 60 Hz Power (H)	115 v 60 Hz Power (H)

Schematic and timing diagrams for the stepping motor limit control are given in Figs. 26 and 27, respectively, of Appendix I.

The RTμL 9900 buffer-driver is connected as a 1-shot multivibrator to generate a buffer loading gate coincident with the trailing edge of the print command from the digital voltmeter. This gate loads the buffer, CμL 9959, with the current state of the under-range and over-range signals from the DVM which stores them until a new print command is received. This

buffer also serves as an interface between the RTL logic levels of the DVM and 1-shot, and the TTL logic levels required by the SN 7407 buffer-drivers. If either the over-range or under-range signal is low, indicating that the corresponding off-scale condition of the DVM exists, then the 3 paralleled sections of the buffer-driver controlled by that signal are turned on shorting the stepping motor controller input pulses to ground thus preventing further motion in the corresponding direction. The resistor in series with each pulse input operates in conjunction with the corresponding zener diode to limit the pulse voltage to a value which will not damage the buffer drivers. This resistor also limits buffer current, and loading of the pulse source, to a safe value when the pulses are shorted to ground by the buffer drivers.

4. Recorder Control Unit

A wiring diagram of the recorder control unit is given in Fig. 28 of Appendix I. This unit contains control buttons and indicators, essentially duplicating those found on the Ampex FR-1400 tape recorder front panel thus permitting operation of the tape recorder from the control console after a tape has been mounted and primary power has been applied. The recorder control unit connects to, and derives all operating power from, the FR-1400 tape recorder via the interconnecting cable shown which mates with connector J211 on the rear of the recorder. The RECORD SPEED indicator on the recorder control unit indicates that the proper recording speed, 120 ips, has been selected via the selector switch on the recorder front panel. The RECORD SPEED ERROR indicator is illuminated if any other speed has been selected. For additional information concerning the operation of the controls and indicators, the manuals furnished by the recorder manufacturer should be consulted.[8]

Two relays, RY1 and RY2 of Fig. 28 are provided within the recorder control unit to provide logic signals indicating RECORD and/or REPRODUCE states of the recorder to the data registers and serial data decoders, respectively, of the scanner logic unit. These relays simply ground the logic line (Pin A or B on P66) via a common return (Pin C) when the corresponding state exists thus producing a logical zero level. When the lines are not thus grounded, a logical one level is produced via returns to the logic supply Vcc through 1 K resistors located in the scanner logic unit.

Also connected to P211 (see Fig. 28) is another 4-conductor cable, which, through an intervening connector shown, connects to P324 on the rear of the recorder. This cable provides signals for automatic selection of the High (120 ips) and Low (15 ips) speed Miller code electronics via the speed selector switch on the recorder front panel. Changes required in the Miller code electronics chassis to achieve this have been appropriately indicated on the manufacturers schematics[9] furnished with the recorder.

5. DC Power Supplies

All dc voltages for the console control unit and scanner logic unit, as well as 24 and 28 volts dc for the scanner and scanner control unit are supplied by the logic power supply LPS-1. A wiring diagram for this unit is given in Fig. 29 of Appendix I. All voltages except for +24 volts are supplied by commercial power supplies as listed in Fig. 29 and in Table VII. The +24 volt output used for various indicators and relays throughout the system is obtained via a series pass transistor and zener reference diode from the unregulated 28 volt supply. A series choke in the base circuit of this transistor, and bypass capacitors across the output, and input and output of the 28 volt supply, suppress high frequency oscillation which could result from stray coupling in this circuit. A chassis-mounted fuse, F7 protects the series transistor in case of accidental grounding of the output.

A crowbar circuit for the -5 volt supply is included on the LPS-1 circuit board. This circuit protects the logic components from damage by shorting the -5 v supply output to ground if the voltage magnitude increases beyond approximately 5.5 volts for any reason. A similar crowbar circuit is included within the +5 volt supply, PS4.[19]

Primary A-C power to all console-mounted components is controlled by the A-C Relay RY1 of Fig. 29, provided that the display indicator, A/D converter, and multiplexer power cords are connected to the 115 v receptacles provided on the rear of the chassis for this purpose. This relay may be operated via the front panel switch, SW2, for test purposes. Normally this switch is set to the REMOTE position, however, and relay operation is controlled by the main power buttons located on the console control unit.

A circuit breaker for A-C power input and indicator fuse posts for the 115 volt power control circuits and for each individual power supply are mounted on the front panel.

DC power for the scanner and scanner control unit is obtained from commercial power supplies as listed in Table VII. (See also the wiring diagrams for these units, Figs. 22 and 24.) One supply, PS1 of Fig. 22, used to power the projector lamps has been significantly modified by adding a voltage crowbar, increasing the delay of the current crowbar so it will not be tripped by initial surge current when lamp filaments are cold, replacement of the voltage reference diode to improve temperature stability, and the addition of a terminal strip and connectors to facilitate wiring of the scanner unit. A schematic diagram for this supply is given in Fig. 30 of Appendix I. All other power supplies are commercial units, as supplied by the manufacturer. For additional information on these units, the manufacturer's literature should be consulted.[15,16,19]

TABLE VII
DC POWER SUPPLIES

Voltage	Current	Regulated	Location	Unit	Mfr. & Type	Use
±15 v	150 ma	Yes	LPS-1	PS1	VDN* DPM 15/150	D/A Converters
±12 v	100 ma	Yes	LPS-1	PS2	PMC MD 12c	Operational Amplifiers
-5 v	250 ma	Yes	LPS-1	PS3	PMC MM5B	Line Receivers & Video Switching
+5 v	10 A	Yes	LPS-1	PS4	PMC ICX 5cc	All Console Logic
+28 v	5 A	No	LPS-1	PS5	APN 28 UBT 500	Stepping Motors, Relays & 24 v Reg.
+24 v	2 A	Yes	LPS-1	Series Reg.from 28 v DC		Indicators & Relays
±15 v	400 ma	Yes	CU-2	PS3	PMC PT 99	D/A Converters &-5v Reg.
±12 v	400 ma	Yes	CU-2	PS2	PMC PT 99	Operational Amplifiers
-5 v	150 ma	Yes	CU-2	Series Reg. from -15 v (on line driver board)		Line Drivers & Video switching
+5 v	4 A	Yes	CU-2	PS1	PMC UNI 30C	All Scanner Logic
+5.5 v	5 A	Yes	Scanner	PS1	WNS 60 OEM-1†	Sync. Projector Lamps
-1250 v	4 ma	Yes	Scanner	PS2	ABT HAK05D-1230 A	Sync. Detectors

*Mfr's. Code: VDN - Varadyne
PMC - Powermate
APN - Acopian
WNS - Wanlass
ABT - Abbott

†Modified - see Fig. 30

6. Scanner Logic Unit

The scanner logic unit SLU-1 is essentially a card cage, with associated cable connectors, housing all console logic cards as previously presented in Fig. 21, Section A, above. Details of the individual circuit cards are given in the following section.

C. Logic Circuits

This section contains the detailed theory of operation for all logic cards contained in the scanner control unit CU-2 and scanner logic unit SLU-1 and certain closely associated components such as the sync detectors and multiplexer-mounted data ready delay. Pertinent details of the multiplexer and A/D converter are also discussed in logical sequence with these circuits. Associated logic and timing diagrams which are frequently referenced throughout this section are located in Appendix I.

Certain logic cards are found both in the scanner control unit CU-2 and in the console-mounted scanner logic unit, SLU-1. Such cards are functionally identical, hence the following descriptions apply to both. However, cards for the scanner control unit are physically larger than those for the scanner logic unit, hence the cards are not directly interchangeable. Also, all cards for the console mounted scanner logic unit utilize 7400 series integrated circuits (as indicated on the logic diagrams) while the corresponding cards used in the telescope-mounted scanner control unit, which could be subjected to wide ambient temperature variations, utilize the more rugged 5400 series integrated circuits.

1. Video Preamps

The video preamps, Fig. 31, are gain controllable IC linear video amplifiers. Two pairs of amplifiers are used, one pair for channel A with input supplied from the A channel Perry Preamp (see Fig. 22) and an identical pair for channel B. The output from one amplifier of each pair is applied via a coupling capacitor to the video switching circuits and then to the scanner control unit CRT display, while the other amplifier of each pair drives a 92 ohm coaxial cable to the control console via an emitter-follower and output coupling capacitor.

Gain control for each amplifier is provided by means of a photomod which consists of a photoresistive cell packaged with a tungsten-filament lamp. By varying the current supplied to the lamp the photocell illumination is varied, and hence its resistance. This resistance is connected to the gain control terminals of the amplifier, hence the amplifier gain is varied. A gain of approximately 10 to 200 is available with this amplifier-photomod combination. Since the photomods provide excellent isolation, no signal currents flow in the gain control leads and the gain controls may be mounted remotely without difficulty. A gain control

for the amplifiers driving the scanner CRT display is provided on the front panel of the scanner control unit. This control is switched to the channel being viewed by the channel selector switch (see Figs. 20 and 24). As shown in Fig. 24, the gain control consists of a variable resistance in series with a 12 volt source which is applied to the photomod lamp filament. The 12 volt source is obtained from the +24 v supply (located in the logic power supply) via a zener diode and dropping resistor.

Independent gain controls are provided for the A and B channel amplifiers driving the coax. cables to the console, since both may be used simultaneously. These controls are located on the console control unit and are similar to that described above (see Fig. 25).

By locating the gain controlled video preamps driving the console in the scanner control unit, a high video signal level can be obtained over the coaxial cable run for a variety of input signal level conditions. This insures that the signal to noise ratio is not significantly degraded by noise pickup by the cables.

2. Sync Projectors and Detectors

As previously described in Chapter II, Section A, three sync detectors are used in conjunction with two sync projectors and the scanning disc to generate synchronization signals for controlling signal sampling during the scanning process, for pre-recording signal processing, and for raster generation for visual display of the recorded and/or on-line sampled images. These components, together with the associated power supplies and voltage divider are shown in the scanner wiring diagram, Fig. 22 and physical locations are given in Figs. 15 and 17.

The sync projectors, one for word sync which projects two 20-line reticles onto the disc, and one for the line, frame, and disc sync which projects a reticle consisting of 3 line segments, are identical except for physical mounting details. Each contains a special square filament projection lamp (Phillips #13347W) powered by the +5.5 v. power supply PS1 of Fig. 22, a condensing lens, reticle holder, and projection lens. Procedures for aligning these projectors are given in Appendix IV.

The sync detectors are basically photomultiplier circuits with appropriate optics to collect light passing through the scanning disc apertures from the reticles. The photomultipliers generate negative-going output pulses from the light pulses thus received. Schematic diagrams for these detectors are given in Fig. 32. The line, frame, and disc sync detector contains a Type 931A photomultiplier. Because of the wider field of view required as well as physical mounting restrictions, the two word sync detectors, which are identical, utilize end-on type 7767 photomultipliers.

The dynode voltage divider strings used with the photomultipliers are designed to cause saturation at high illumination limiting photomultiplier anode current to approximately 350 μa maximum. This protects the photomultipliers from damage and also protects the operational amplifiers and Schmitt triggers of the scanner sync generator (see below) from damage due to excessive applied voltage in the event of high ambient illumination. A 2K ohm load resistor is mounted inside each detector housing and another, connected in parallel, is mounted on the scanner sync generator PC board, hence neither circuit will be significantly disturbed or damaged if the photomultiplier output cable is disconnected with power applied. The net load impedance for each photomultiplier is therefore 1K ohm and the maximum (saturated) output voltage applied to the scanner sync generator input is approximately 350 millivolts.

3. Scanner Sync Generator

A logic diagram for the scanner sync generator is given in Fig. 33 and a timing diagram in Fig. 34. The output of each sync detector is applied to the inverting input of an operational amplifier (CA 3038) operating in the comparator mode (i.e., no feedback resistor is used giving very high gain, hence the amplifier is either on or off) while a reference voltage is applied to the noninverting input from a voltage divider connected to the -5 volt supply. A potentiometer in the voltage divider permits setting the trigger point for the comparator amplifier at a point on the input waveform where the slope is steep (for reliable timing) and where noise or variations in input signal amplitude will not cause false or erratic triggering. The comparator amplifiers are operated from symmetrical 5 volt supplies and a diode clamp is included between pins 2 and 11 of each amplifier to prevent the output from going negative in order to provide proper voltage levels for the Schmitt triggers which follow.

The primary purpose of the Schmitt triggers (SN 5413) is to provide TTL compatible voltage levels for the remaining circuitry; however, they also serve to further shorten the rise time of the signal waveforms.

Each Schmitt trigger output is applied to trigger a one-shot multivibrator (SN 54121) which produces a narrow output pulse approximately 120 ns in width coincident with the leading edge of each input pulse. For line, frame, and disc sync this output pulse train is the required sync signal waveform. The even and odd word sync pulse trains (taken from the $\overline{Q}$, or inverse, outputs of the 1-shots) are ORed together via a NAND gate (SN 5400), the output of which is the required Channel A raster word sync pulse train. These sync signals are used in the scanner control unit to generate a raster for visual display and are also sent via the line drivers (see below) and coaxial cables to the console-mounted scanner logic unit (see Fig. 20).

4. Line Drivers

A schematic diagram of the line driver PC board is given in Fig. 35. The line drivers, type SN 55109, accept TTL logic level inputs and provide low impedance high current outputs suitable for driving the 100 ft. coaxial cables connecting the scanner logic unit to the control console. Two IC packages are used, each containing two identical, independent line driver circuits. Only one circuit of each package is used at present leaving the other two as spares.

The output capacitors (.0013 μfd.) are chosen to match the total distributed capacity of the cable used. If cable length and/or type is changed, these capacitors should be changed also (see Note, Fig. 35) for most reliable, noise-free operation.

A -5 v supply is required for the line drivers in addition to the normal +5 v logic supply. Since no separate -5 v power supply is provided in the scanner control unit, -5 volts is obtained from the -15 volt supply via a series-pass transistor (2N 2905) and zener reference diode (IN 752A). This circuit also supplies -5 volts to the scanner sync generator (see above) and the video switching and D/A converter cards mounted in scanner control unit (see Fig. 20).

A -5 volt crowbar circuit similar to that described earlier for the logic power supply LPS-1 (see paragraph B-5 above) is also included to protect the components connected to the -5 v line in the event of a shorted series-pass transistor or other failure resulting in abnormally high voltage on the -5 v line.

5. Video Filter Amplifiers

The console-mounted video filter amplifier circuit board, shown schematically in Fig. 36 contains two identical amplifiers, one each for A channel and B channel video. Each amplifier provides a matched termination for the coaxial video cable from the scanner control unit video preamplifier and provides a matched output sufficient to drive the video filter, multiplexer, and A/D converter to full scale output. Each amplifier consists of a type CA 3038 operational amplifier connected in a high current output, inverting configuration. A relay and 25.5 K ohm resistor in parallel with the 100 K feedback resistor for each amplifier provide gains of approximately 2 and 10, selectable by means of the corresponding HI-LO gain switch mounted on the console control unit front panel (see Fig. 25).

6. Video Filters

The video filter board, Fig. 37, contains identical low-pass filters for A channel and B channel video to restrict the channel bandwidth to that required by the signal. Thus any higher frequency noise components introduced by the wide band video amplifiers and/or picked up by the cables are removed prior to sampling. Such noise components, if present, are of little consequence in an analog video display since they are effectively filtered out by the persistance of vision of the observer, if not by the CRT phosphor decay time. They must be removed prior to sampling however, or they may appear as extraneous signals in the sampled data (i.e., aliasing) since the Nyquist sampling criteria (requiring a minimum of 2 samples per cycle for all frequency components present) would be violated with respect to these signals.

The low pass filters are of the 4-element Butterworth type, and are essentially flat to 160 KHz, the highest legitimate signal frequency present, with roll off to -3 dB at 430 KHz and -67 dB at 3 MHz.

7. Line Receivers

A schematic diagram of the line receivers is given in Fig. 38. As for the line driver board described previously (paragraph 4 above) two IC packages (type SN 75107) are used, each having two independent circuits. One circuit of each package is presently used while the others are spares.

The line receivers convert the sync signals received from the line drivers via the coaxial cables to TTL compatible logic levels for use throughout the scanner logic unit (see Fig. 21).

The input capacitors (.0013 μfd.) are chosen to match the total distributed capacity of the line used. If cable lengths and/or type are changed, these capacitors should be changed also as indicated in the Note, Fig. 38, for most reliable, noise-free operation.

8. Sync Separator

The composite line, frame, and disc sync pulse train is separated into individual outputs by the sync separator, Figs. 39 and 40. Each output has an independent time delay adjustment so that small variations in input pulse timing from the correct values can be compensated electrically and mechanical adjustments of the line, frame, and disc sync projector and detector are therefore much less critical.

A line sync pulse is present preceding every image line and occurs first in the input pulse train (see timing diagram, Fig. 40). This pulse is applied via the upper NAND gate of Fig. 39 to trigger the line sync delay 1-shot which, after an adjustable delay of 9 μs (nominal) triggers the line sync 1-shot thus generating the required line sync output pulse.

The lower two NAND gates are gated off during the duration of the 1st input pulse. The trailing edge of this pulse, however triggers the frame sync gate 1-shot which then, for an 8.9 μs interval, gates on the center NAND (Fig. 39) while gating off the other two. If another input pulse (which is present preceding every image frame) occurs during this interval it then triggers the frame sync delay 1-shot which, after a nominal 6 μs delay generates a frame sync output pulse via an additional 1-shot, as above.

The trailing edge of the frame sync gate 1-shot then triggers the disc sync gate 1-shot for an interval of 6 microseconds which gates on the lower NAND while gating off the other two. An input pulse (present preceding every second frame - i.e., once per disc rotation) occurring during this interval thus triggers the disc sync delay, and after a nominal 3 μsec delay produces a disc sync output pulse via the corresponding 1-shot.

As mentioned previously, the individual delays are adjustable, and should be set to produce the proper output pulse timing with respect to the Channel A raster word sync pulse train as shown in Fig. 40.

9. B-Sync Generator and Digital Data Demultiplexer

Several additional synchronization signals which can be derived from the Channel A raster word sync and A line sync signals (see paragraphs 3 and 8 above) are required throughout the system (see Fig. 21). These signals, B raster word sync, B line sync, A data register line sync, B data register line sync, channel address, and channel transfer, are obtained via the B-sync generator. Closely related signals, A data strobe and B data strobe, are also required for demultiplexing the digital data following analog multiplexing and A/D conversion. These are generated from the present channel address and data ready signals from the multiplexer and A/D converter, respectively, by the digital data demultiplexer mounted on the same circuit board. A schematic diagram of these circuits is given in Fig. 41, and the corresponding timing diagrams in Figs. 42 and 43. Additional information concerning the requirements and derivation of the various word sync related waveforms generated by these circuits is given in Appendix II.

The Channel B line sync and raster word sync signals are obtained from the corresponding Channel A signals via a delay equal to ½ the word spacing of the shortest raster line. This delay is provided by the B-channel delay 1-shot (see Figs. 41 and 42) which is triggered by each A line sync or A raster word sync input pulse. Output pulses of approximately 120 ns duration are generated following each delay gate by the B-delay pulse generator 1-shot. The A line sync input pulse also sets the A data register line sync flip-flop while the first A raster word sync pulse clears this flip-flop generating the required output waveform having a negative-going transition coincident with the first word sync pulse of each data line. The outputs of this flip flop are also used in conjunction with the two upper AND gates of Fig. 41 to

demultiplex the B line sync pulses and B raster word sync pulses onto separate output lines.

The B line sync and B raster word sync waveforms are then used to generate the B data register line sync output via an additional flip-flop as was done for A channel, above.

The channel A and channel B raster word sync pulses (used by the raster generators for analog video display) occur at the beginning of each data word interval (i.e., just as the disc begins to scan the corresponding image element). Sampling for A/D conversion however should occur at the center of each image element and, since a single A/D converter is used for both channels, samples from the two image channels must be multiplexed. Generation of the required waveforms, channel transfer to initiate sampling, and channel address to designate the channel to be sampled, will now be described.

The A raster word sync and B raster word sync pulse trains are individually delayed (by ½ the word spacing of the shortest data line minus the multiplexer set-up time) by means of the A channel transfer delay 1-shot and B channel transfer delay 1-shot, respectively, and their associated pulse generator 1-shots. These are then ORed and inverted by the NAND gate to produce the required channel transfer waveform. The channel address waveform is obtained from the channel address flip-flop which is set and reset, respectively, by the B channel transfer delay and A channel transfer delay 1-shots.

Digitized samples for both A and B channel video appear, multiplexed, on the 8 A/D converter output data lines (see Fig. 21). These are demultiplexed by strobing the data from the lines into the appropriate registers or other circuits via the A data strobe or B data strobe, as required. These strobes are generated by the digital data demultiplexer which consists of the three lower logic gates of Fig. 41. The data strobes originate as the data ready pulse generated by the A/D converter each time a new sample is available on the data output lines. This pulse is routed to either the A data strobe or B data strobe output line via the two AND gates, and NAND inverter, driven by the present channel address waveform from the multiplexer. These waveforms are given in the timing diagram, Fig. 43.

10. Co-ax Driver

Since the standard TTL logic circuits used throughout the system are not directly capable of driving lines more than a few inches in length, line drivers are required to drive the interconnecting coaxial lines to the multiplexer and tape recorder (see Fig. 21). As shown by the schematic diagram, Fig. 44, each line driver consists of three parallel sections of a type 7407 non-inverting, open collector buffer-driver IC, with collectors returned to Vcc via a 47 ohm resistor. Each driver is capable of driving a 93 ohm coaxial cable at least 25 ft in length provided the cable is properly terminated in a matched load at the

receiving end. Eight identical driver channels are provided on the circuit board. Four terminated "feed-throughs" are also provided on this board for signals received via coaxial cable from the multiplexer and A/D converter.

11. Multiplexer

The multiplexer is, except for one modification described below, a standard commercial unit, and for operational details the manufacturer's manual should be consulted.[20] This multiplexer, a two-channel version of the Computer Labs Model MUX-810 is capable of multiplexing the analog video signals from the two input channels for subsequent sampling and analog to digital conversion at a rate up to 2 megawords per second. Next channel address and channel transfer signals (see paragraph 9, above) are supplied to the multiplexer to initiate switching the desired analog input signal onto the output line. Switching is accurately completed (including settling time) so that A/D conversion of the new data sample may begin approximately 200 ns after receipt of the channel transfer pulse.

As received from the manufacturer, the channel transfer pulse applied to the multiplexer input connector was simply paralleled off via the channel ready output connector to signify that the multiplexer had completed the transfer; whereas, as stated above, the switching process is not actually completed until 200 ns later. Hence, in order that the A/D converter does not begin conversion prior to arrival of the correct input signal a 200 ns delay has been added between the channel transfer input signal and channel ready output as shown in Fig. 45. This circuit, which consists of a 200 ns (adjustable) delay 1-shot followed by a pulse generator 1-shot (120 ns nominal width) and output driver for 93 ohm coaxial cable, is installed inside the multiplexer. A connector has been installed and appropriately wired for this purpose in the card slot position originally intended for the channel 8 analog data switching circuit which was unused since the multiplexer is equipped with only two input channels.

In addition to the analog data output and data ready signals which are sent via coaxial cables to the A/D converter, the multiplexer also furnishes a present channel address signal to the system logic (see paragraph 9, above), indicating the channel presently selected, which is used for subsequent demultiplexing of the digital data as previously described.

12. A/D Converter

The analog-to-digital converter is an 8-bit, parallel output, standard commercial unit (Computer Labs Model HS-802) having a maximum conversion rate of 2 megawords per second. Specifications, operational and circuit details, and schematic diagrams are given in the manufacturer's manual[21] supplied with the equipment which should be consulted for additional information.

The analog input signal, and encode command which initiates sampling and conversion of a new data point, are supplied by the multiplexer. The encode command input is simply the channel ready output from the multiplexer as described in the preceding paragraph. Approximately 125 ns after receipt of the encode command signal the new digital data is available on the 8 data output lines. At this time the A/D converter furnishes a data ready pulse to the system logic which, via the digital data demultiplexer (see paragraph 9, above), is applied to strobe the data from the lines into the data registers of the A and B channel parallel input-serial output encoders described below.

13. Parallel Input-Serial Output Encoder

Digital video data available from the A/D converter is in parallel, 8-bit binary form. In addition, because of the scanning method used (see Chapter II), the data is asynchronous. As discussed previously (Chap. II) parallel recording on separate tracks at the required data rate is not feasible because of dynamic skew limitations, hence a high density serial recording (Miller Code) technique utilizing a single magnetic tape track for each video channel is used. The required format which combines video, sync signals, and an optional parity check in a single, synchronous, serial data stream for application to the Miller Code system has been given previously in Fig. 7, Chapter II. The purpose of the parallel input-serial output encoder is to generate this serial data stream from the available input data and sync signals.

Two identical parallel input-serial output encoders are provided, as shown in Fig. 21; one for each data channel. Each encoder consists of three circuit boards, and in addition, certain auxilliary circuits used by both channels (see paragraph 14, below) comprise one additional board. A logic diagram of the encoder is given in Fig. 46 and corresponding timing diagrams in Fig. 47.

The basic function of the encoder is to convert the asynchronous parallel input data, plus synchronization signals required for raster generation at playback, to a synchronous serial bit stream suitable for the Miller code system. This is accomplished by means of six 8-bit parallel input-serial output shift registers, each consisting of two serial connected type SN7494 IC's (see Fig. 46). Five of these registers, mounted on decoder board #2, are used for data storage and conversion (or gap filler 0101 code if data is not available) while the sixth, mounted on decoder board #3, is used for inserting the 4-bit preamble and 4-bit sync code (see Fig. 7) into the serial data stream as required. The remaining logic circuits of the encoder control the loading and unloading of these registers, provide switching for the optional parity check mode, generate parity when this mode is used, and provide appropriate start and stop sequences for the decoder when the recorder is switched on and off, respectively.

Since data input is asynchronous (i.e., data for each image line comes in a burst at an input frequency peculiar to that particular line

(but exceeding the output data rate), followed by a gap of varying length prior to arrival of data for the next line) while data output is synchronous, temporary data storage must be provided within the encoder. This is provided by the five data registers. These are loaded in sequence as input data arrives; and are unloaded, in sequence, at a constant rate determined by the output data clock (see paragraph 14). For the input and output data rates used for this system, 5 data registers are sufficient to insure that at least one empty data register is available whenever input data arrives, even allowing for possible variations in scanning speed (determined by the instantaneous speed of the synchronous scanning disc motor).

For a continuous system such as this, average input and output data rates must obviously be identical. Also, the output bit rate must be a known constant in order for the Miller code system to function properly. These requirements are met while still permitting small variations in scanning speed via the variable length 0101 gap filler code of Fig. 7. Since the 101 sequence is used by the Miller code system at playback to recover the data clock from the recorded data, this gap filler code, together with the preamble (Fig. 7) and any 101's occurring in the video data, also helps insure proper clock synchronization during playback.

Operation of the data encoder will now be described with reference to Figs. 46 and 47.

The 8 parallel data input lines (or 7 data lines plus parity bit for the parity check mode) are hard wired to the data 1 inputs of all 5 data registers. Channel A and Channel B video data are multiplexed on these lines as discussed previously (paragraphs 9, 11, and 12, above). The appropriate register is parallel loaded with this data by strobing the preset 1 input of that register when the desired (Channel A or Channel B) data is present on the input lines. The required data strobe enters the encoder (board #1) from the digital data demultiplexer (paragraph 9), is delayed by 40 ns (i.e., the width of the input pulse) and lengthened to 100 ns by the data strobe delay 1-shot, and is then routed to the appropriate register preset 1 input via the data in decoder under control of the input address counter. The delay is required to insure sufficient time for generating the parity bit prior to loading.

The data 2 inputs of all data registers are hard wired for 0101 (gap filler) code. This code may be loaded as desired by strobing the preset 2 input of the appropriate data register. A strobe for this purpose is generated by the 0101 decoder strobe 1-slot (board #1), provided that the 0101 loader is enabled (see below), each time the data output address advances to the next register. This strobe is routed to the appropriate register by the 0101 decoder which is also controlled by the input address counter, as above.

The data 1 inputs for the first 4 bits of the sync register (board #3) are hard wired for the 0101 preamble (Fig. 7) which may be loaded by strobing the preset 1 input. The data 2 and preset 2 inputs for this half of the register are not used. Data 1 inputs for the last 4 bits of the sync register are hard wired for the line sync code (0000) which is loaded simultaneously with the preamble via the preset 1 input, while the data 2 inputs for these bits are supplied with frame sync code (either 0011 or 1100 depending upon the mode selected) which may be loaded by strobing the preset 2 input.

Assume that the system is in steady state operation and is, at the moment, clocking out gap filler code after completing the data output for the previous line (a process which will be described later). The loading sequence for the new data line is then as follows:

A line sync pulse is first received indicating that data words for the new line will be available within several microseconds (see Fig. 47, sheet 1). This pulse is applied to the preset 1 input of the sync register thus loading the preamble and line sync code. If the new line also happens to be the beginning of a new frame, a frame sync pulse is received approximately 3 μs after the line sync pulse. This pulse is then applied via the frame sync code preset 1-shot (which provides a 120 ns delay required during system turn-on or mode switching) to the sync register preset 2 input thus changing the line sync code previously loaded to frame sync code. This register is now available for output.

Next, the trailing edge of the data register line sync pulse is received which triggers the data ready 1-shot. The output of this 1-shot then resets the input address counter to 000, resets the 0101 decoder strobe flip-flop which in turn gates off the 0101 loading logic thus preventing further loading of gap filler code into the data registers, and enables the output reset flip-flop. This flip-flop is concerned with data output and will be described later.

The first data strobe for the new data line then arrives and is applied, via the data strobe delay 1-shot and the data in decoder, to the preset 1 input of the 1st data register (address 000) thus loading the 1st data word into that register; the trailing edge of the data strobe increments the input address counter to select the next register (address 001) for the next data word. Subsequent data strobes thus load the remaining data words of the line into the data registers in sequence. Since the input address counter is of the divide by 5 type, it automatically recycles back to 000 after the 5th data register (address 100) has been loaded and the cycle is repeated for data words 6 through 10, etc., until all 40 data words of the line have been loaded. Note, as mentioned previously, that input and output rates are such that data word 1 will have been unloaded from the 1st data register before that register is again required (for data word 6), etc., so that no overlapping of data occurs.

After all 40 data words of the line have been loaded an 0101 loader enable pulse is received from the line length counter and gate located on the data register clock board (see paragraph 14, below). This pulse sets the 0101 decoder strobe flip-flop enabling the 0101 loader logic so that, from this point on, whenever the output address counter is incremented to output data from a new register, the register currently addressed by the input address counter (i.e., the register immediately following the last register previously loaded) will be loaded with gap filler code. This is accomplished, as mentioned previously, by applying the output of the 0101 decoder strobe 1-shot, via the 0101 decoder, to the register preset 2 input. The trailing edge of the 1-shot output pulse is also now applied to increment the input address counter preparatory to loading of the next gap filler code word, if required.

Since the instantaneous data loading rate (during the time when a data line is being received) exceeds the instantaneous data output rate (a constant), a surplus of data is always available in the registers immediately after loading the last data word of each line. Thus the need for gap filler code is not immediate and loading of this code can await the advance of the output address counter to the next register, as described above. With this method of loading gap filler code, the average loading rate is identical to the unloading rate so that the time interval for which gap filler code can be supplied is unlimited. (This is important during system turn-on, as will be described later.) The loading cycle is now complete, and with the arrival of the next line sync pulse to the encoder, the cycle is repeated.

The data encoder output sequence will now be described. Data is clocked out serially from each data register by applying a clock input to that register. A new data bit appears at the output each time the clock input goes positive. As data bits are clocked out, zero bits are clocked in (since the serial input to each register is grounded), hence 8 clock cycles are sufficient both to serially unload the register of all data contained therein, and to clear the register to zero which is required prior to subsequent parallel loading.

The 2.716 MHz data clock is received from a crystal controlled clock oscillator and divider (see paragraph 14 below) and is applied via an inverter and the data out decoder, under control of the output address counter, to the clock input of the data register to be unloaded. The output of this register is simultaneously connected to the output data line by the output data selector, also controlled by the output address counter. The output address counter is driven by a divide-by-eight bit counter (since there are 8 bits per data word) which is in turn driven by the data clock.

The output address counter is basically a divide-by-five counter, similar to the input address counter, which automatically cycles (000 through 100 and repeat) thus addressing the five data registers in succession when incremented by the address clock (bit counter output).

AND gating from the A and D outputs to the A input, and OR gating from the A and B outputs to the low order bit output line have been added however which modify the operation of the counter in the following manner: A reset pulse applied to the R9 inputs of the counter will set the counter output to 101 thus addressing the sync register. Successive input pulses will now cause the counter to step to 000 and then continue cycling (000 through 100) as a divide-by-5 counter, never again reaching the count of 101. Hence, by means of the R9 reset, this counter may be used to automatically include the contents of the sync register at the beginning of the first output cycle for each data line, and then to exclude it during output of the remaining data and gap filler code.

Now assume the system to be in steady state operation with 0101 gap filler code being clocked out as before. Further assume that line sync, and frame sync, if present, have been received thus loading the sync register, and that the trailing edge of the data register line sync pulse has been received enabling the output reset flip-flop via the data ready pulse from the data ready 1-shot as previously described. Upon completing the output of the current 01 bit sequence of the gap filler code which may be in progress when the output reset flip-flop is enabled, the leading edge of the B output from the bit counter is applied via an inverter to set the output reset flip-flop. The output of this flip-flop in turn triggers the output reset 1-shot which generates reset pulses to reset the bit counter to zero, clear the 5 data registers prior to loading new data, and set the output address counter to 101, thus addressing the sync register, via the R9 reset inputs as described above. The first bit of the preamble from the sync register is then immediately available at the data output line of the encoder and successive bits of the preamble and sync code then follow, synchronous with the data clock. When all bits from the sync register have thus been unloaded the output address counter will be incremented to 000 by the address clock and data bits from the 1st data register, which will have been loaded prior to this time, will then be clocked out. The output sequence then continues cycling through the 5 data registers in succession clocking out all data for the line, and will then continue to clock out the 0101 gap filler code loaded into successive data registers following the data input cycle as previously described. This process continues until the next data ready pulse occurs initiating a new output cycle for the next data line.

The above descriptions of the input and output sequences assume steady state operation. If the first data frame recorded after turn-on is to be recoverable during playback, three additional requirements must be met: (1) some means must be provided for synchronizing the Miller code output data clock at playback prior to arrival at the 1st actual data, (2) data recording must start at the beginning of a data frame, and (3) all registers and counters must be reset prior to inputting the first data frame to the encoder.

The requirement for clock synchronization at playback is met by recording a series of 0101 sync code for a period of approximately 5 seconds following recorder turn-on prior to recording of the first data frame. The start of actual data recording is triggered by arrival of a frame sync pulse, hence data recording always begins at the start of a new frame; and finally, proper reset of the registers and counters prior to loading of the first data frame is assured by clocking out and reloading the sync register and by resetting the counters and clearing the data registers via the output reset 1-shot as for steady state operation. A system clear 1-shot to clear all counters and data registers following recorder turn-on has also been included during development of the encoder, but actually is not required during normal operation of the present system. Operation during recorder turn-on will now be described with reference to Fig. 46 and Fig. 47, sheet 3.

Prior to recorder turn-on the encoder operates as in steady state with input and output exactly as previously described. The output is, of course, not being recorded, but it may be viewed on the visual display indicator if desired by setting the selector to the SERIAL IN position. If the two RECORD buttons on the recorder front panel or recorder control unit are now pressed, the tape will accelerate to recording speed and the pinch rollers and recording heads will then close. At this time the record relay in the recorder control unit (Fig. 28) will close. Contacts of this relay are indicated by the Recorder off-on switch of Fig. 46, and as shown in this figure, the on position applies a 0 level to the on-off flip-flop D input so that this flip-flop is reset when the next frame sync pulse arrives. The output of this flip-flop triggers the system clear 1-slot thus clearing all data registers, the sync register, and output address counter to zero; and setting the input address counter to 100 (functions not actually required in the present system, as mentioned above). It also triggers the 5 second start-up delay 1-shot. During the timing cycle a 0 level is applied to the D input of the data enable flip-flop by the 1-shot. When the next frame sync pulse occurs the data enable flip-flop is reset. The output of this flip-flop is applied to disable the frame sync code preset 1-shot, gate off the data strobe input, and force a set state, via the input gates, for the 0101 decoder strobe flip-flop thus insuring that 0101 gap filler code only is loaded into the data registers during the remainder of the timing interval. Reset of the output address counter and input address counter is also prevented during this interval by gating off the data ready pulse via the input AND gate to the 0101 decoder strobe flip-flop. Thus, the decoder supplies a continuous train of 0101 gap filler code to the recorder during the remainder of the 5 second start up delay.

Note that during the 1 frame interval (5 ms) between reset of the on-off flip-flop and reset of the data ready flip flop the sync register will have been clocked out (40 times, in fact) thus clearing it to zero (via the grounded serial input) insuring that no stray bits are present in this register. It also will have been reloaded (40 times) with preamble and line sync code in preparation for outputting the 1st data

frame at the end of the start-up delay. Since line sync input to the data register is not inhibited during the start-up delay, the sync register loading cycle will be repeated many times during the remainder of this interval, but will not change the contents of the sync register. The frame sync code preset 1-shot has been inhibited however, so that frame sync code will not be loaded. This is important because frame sync code depends upon the recording mode selected, and mode could be switched by the operator during the start up delay resulting in incorrect sync code for the 1st data frame if this code were preset. (Note that while it is possible to change line sync code to frame sync code by preset alone (no clear cycle) it is not possible to change frame sync code in this manner since the preset operation will change 0's to 1's, but not 1's to 0's.)

At the end of the start up delay a 1 level is again applied to the D input of the data enable flip-flop and when the leading edge of the next frame sync pulse occurs, this flip-flop is set returning the system to normal operation. The trailing edge of this frame sync pulse triggers the frame sync code preset flip-flop thus loading the frame sync code in the sync register which already contains preamble and line sync code (see above). The data ready pulse then initiates output of the preamble, sync code, and fist data line as previously described for steady state operation.

When the RECORD mode is turned off (either by the operator, or when end-of-tape is reached) a true level is applied to the D input of the on-off flip flop which then sets when the next frame sync pulse arrives thus completing the on-off cycle. No other change in encoder operation occurs at this time and the encoder output, though no longer being recorded, can still be viewed on the visual display indicator as desired.

A mode selector switch which may be used to select 8 data bits per word, or 7 data bits plus parity, for recording is located on the front panel of the console control unit. This switch, shown schematically in Fig. 46, sets the D input of the mode flip-flop to 1 or 0 for the 7 bit + parity mode or the 8 data bit mode, respectively. Coincident with the leading edge of each frame sync pulse, the D input of the flip-flop is clocked to the output and remains until a subsequent change in D input followed by a frame sync (clock) pulse occurs. Thus the position of the mode switch may be changed at random, but actual switching of the encoder logic will only occur prior to the beginning of a new frame so that no errors are introduced by changing the position of the mode switch while recording is in progress. Timing diagrams for mode switching are given in Fig. 47, sheet 3. Note that loading of the frame sync code (which is determined by the mode selected) is delayed until the trailing edge of the frame sync pulse occurs (via the frame sync code preset 1-shot) as previously mentioned so that the proper code will be loaded for the frame immediately following a change in mode, as well as for all subsequent frames.

The outputs of the mode flip-flop are applied to the data 2 inputs of the sync register to provide the proper frame sync code for each mode (see Fig. 7), and to the gating inputs of an AND-NOR (SN 7450) used to select either the least significant data bit or the parity bit for the eighth bit applied to the data register inputs. The parity bit is generated from the 7 higher order data bits by means of a parallel input parity generator IC (SN 74180) wired to generate even parity. Note, however, that the AND-NOR used to select this bit produces a data inversion so that odd parity is actually output by the encoder when the 7 bit plus parity mode is selected and, when the 8 data bit mode is selected, the least significant data bit is inverted. The data is recorded in this manner, but the inverted bit is reinverted by the decoder during playback.

14. Data Register Clock and Output Buffer

The data register clock and output buffer PC board, which also contains a line length counter and gate, is used in conjunction with the parallel-input-serial output data encoders described in paragraph 13. A logic diagram of the circuits contained on this board is given in Fig. 48.

The master clock oscillator for the output data clock used by the encoder is a crystal controlled 5.432 MHz oscillator (Vectron Model CO-231) operating from 5 v d.c. and having a TTL compatible output waveform. The oscillator output is divided by two by the SN 7474 flip-flops (one for each channel) to yield the 2.716 MHz symmetrical square wave data clock signals required by the encoders and also by the Miller code recording system. These clock waveforms are also applied to clock the output data buffers which will now be described.

The output from the parallel input-serial output encoders comes, at various times, from 5 different data registers and a sync register which are addressed and selected in sequence by an output address counter and output data selector (see paragraph 13, above). Since the total propagation delays associated with all possible data paths are not identical there is a certain amount of phase jitter present in the data output of the encoder which would cause a significant increase in error rate of the Miller code recording system. It is the purpose of the output buffers (one for each channel) to remove this jitter and furnish a data waveform which is phase coherent with the data clock to the Miller code encoder. This is done in the following manner. The data input (output of the parallel input-serial output encoder) is applied to the D input of a flip-flop (SN 7474). At the middle of each data word interval, when each bit is certain to be present regardless of the input phase jitter, the input is clocked to the output by the positive-going edge of the data clock; hence the data output is phase coherent with the data clock as required by the Miller code system.

As mentioned previously (paragraph 13), the parallel input-serial output encoders require an 0101 loader enable pulse to indicate the end of a data line and initiate loading of the 0101 gap filler code. This pulse is supplied by the line length counter and gate mounted on the data register clock and output buffer PC board. The counter, consisting of 2 type SN 7493 binary ripple counter IC's, is reset by the channel A line sync pulse and then counts the Channel B data strobes (one for each data word) which are applied to the counter input. When the full count of 40 words per line (as selected by the line length jumpers) is reached the NAND gate (type SN 7430) initiates the required 0101 loader enable pulse which is later terminated by reset of the counter (thus removing the required gate inputs) when the next A line sync pulse occurs. Timing of the 0101 loader enable pulse is such that is can be used by both the A channel and B channel data encoders.

15. Magnetic Tape Recorder

The magnetic tape recorder is a standard Ampex type FR-1400 instrumentation tape recorder fitted with 2 channels of Miller code recording and playback electronics for the two data channels and one channel of direct record electronics for recording a 200 KHz sinusoidal signal (control track) used for tape speed servo control during subsequent playback for data reduction on the FR-1900 recorder located at the OSU ElectroScience Laboratory. The Miller code electronics are currently installed in recorder Channels 3 (Channel A video) and 5 (Channel B video) and the control track recording electronics in Channel 1. Other channels could be used as well, except that the FR-1900 recorder used for data playback is presently equipped only with odd-stack heads (i.e., Channels 1, 3, 5, and 7).

Except for the control track oscillator, all recorder components including Miller code encoders and decoders are part of the Ampex recorder system, and are described in detail in the manuals supplied by the manufacturer.[8,9] The control track oscillator, shown in Fig. 49, consists of a Fork Standards Model PQ 200 KHz crystal oscillator and series output level potentiometer mounted on a PC board which is plugged into card slot 1 of the recorder Miller code electronics card cage. The oscillator output is coupled to the recorder control track input via a coaxial cable jumper on the rear of the recorder.

The only other modification to the Ampex recorder system electronics is the installation of matching resistors on the Miller code encoder PC boards to properly terminate the 93 ohm coaxial cables supplying video data and data clock signals to the recorder.

Four 93 ohm coaxial cables supply Channel A and Channel B video data and data clock signals from the scanner logic unit to the recorder for data recording, and 4 additional cables return these signals to the scanner logic unit during playback as shown in Fig. 21. Matched terminations are not required on these latter four cables (which terminate at the serial data decoders) since the cable drivers (located on the Miller code decoder boards in the tape recorder) are matched.

16. Serial Data Decoder

A logic diagram of the serial data decoder is given in Fig. 50 and corresponding timing diagrams in Fig. 51. The purpose of the decoder is to convert the serial data stream, and data clock, from the Miller code recorder during playback (or directly from the parallel input-serial output encoder prior to recording) to parallel data, to extract sync signals from the data stream with proper timing for raster generation, to determine the mode (8 data bits or 7 bits + parity) used during recording, and, if the parity check mode was used, to perform a parity check on the decoded data. Two identical serial data decoders are used in the system, each supplying one of the two identical display indicator channels.

A data selector (type SN 74153) is used at the input to the decoder (See Fig. 50) to select, via the video selector and channel selector switches mounted on the console control unit, any one of 4 pairs of input data and data clock signals which are: Channel A or Channel B Serial In (input signals to the recorder from the parallel input-serial output encoder) and Channel A or Channel B Serial Out (output signals from the recorder).

The selected data clock input is applied to a 1-shot which generates a narrow pulse (30 ns nominal width) coincident with the negative-going edge of each clock pulse (i.e., in the middle of each data bit time interval) which is then used to drive a shift register and counter. The shift register, consisting of two SN 7495 IC's in series, connected for serial input - parallel output right-shift operation, is supplied with the selected serial data and serves as the serial input to parallel output data converter. The bit-counter basically provides a means of counting the 8 data bits per word and provides an output signal indicating that another data word is in position for output. Some means must be provided for synchronizing this counter with the beginning of each data word, however, and for separating data words from preamble, sync code, and gap filler code also contained in the input data stream (see paragraph 13 and Fig. 7), which is the purpose of much of the remaining decoder logic.

Outputs of the first 4 bits of the shift register are applied to the inputs of the 3 sync detector NAND gates, through inverters as required. One of these gates will produce an output whenever the corresponding sync code bits (0000 = line sync; 0011 = frame sync code, 8 data bit mode; 1100 = frame sync code, 7 bit + parity mode) are present in the first 4 positions of the sync register. A fourth gate to detect 0101 gap filler code is also present for test purposes but serves no other function. As previously stated, each of the three sync codes can be precisely located (i.e., the detector produces an output when these 4 bits are completely loaded, but not prior to this time) within the data stream since they are known to always follow an 0101 sequence. Thus an output from one of the sync detectors can be used as a time reference (counter reset) for dividing the data bits which follow into 8-bit data words.

If the sync disable flip-flop is reset (see below) an output from one of the sync detectors will pass through the corresponding NOR gate and other associated logic elements to trigger the line sync 1-shot and thus produce a line sync pulse for output. The line sync 1-shot also clocks the sync disable flip-flop which, assuming that the decoder is active via a true level applied to the D input (see below), will set at this time disabling the sync detectors via the associated NOR gates, enabling the bit and word counters, and enabling the word sync output NOR gate.

If the sync code detected was one of the two frame sync codes (i.e., produced an output from one of the 2 lower sync detector NANDS of Fig. 50) then the frame sync 1-shot is also triggered by the associated logic elements thus producing a frame sync pulse for output. Note that this frame sync pulse, when present, is not coincident with the line sync pulse, but is, in fact, triggered by the trailing edge of the line sync pulse (with the sync disable flip-flop and associated NOR gates) and hence occurs following the line sync pulse as required by the raster generator used for visual display. An output from the 0011 or the 1100 frame sync NAND also is applied (when enabled) to clear or set, respectively, the mode flip-flop thus automatically selecting the 8 data bit mode, or the 7 bits + parity (parity check) mode for decoder output depending upon the mode used during recording.

Data clock pulses, coincident with data bits, received after one of the sync codes has been detected as above will trigger the bit counter. After 8 bits have thus been counted the first data word will be positioned in the shift register ready for output, and an output from the divide-by-eight bit counter will trigger the word sync 1-shot producing a word sync output pulse which may be used, as desired, to strobe the data word into an appropriate buffer (see paragraph 17, below). This process continues, with a data strobe being produced every 8 bits, until the remaining data words of the line have thus been converted for output.

As mentioned above, the sync code detectors are gated off following detection of a sync pulse and must remain off during output of the data line. This is necessary because the data itself may contain bit sequences identical to the sync codes at random locations and such sequences would otherwise be detected as sync pulses producing extraneous outputs from the decoder. Hence it is necessary to detect the end of the data line so that the sync detectors can again be enabled prior to arrival of sync code for the subsequent line. This is accomplished via the word counter and gate (Fig. 50).

The word counter is an 8-stage binary ripple counter driven by the bit counter. The word counter outputs indicate the number of consecutive output data words per line that have been converted to parallel form via the shift register and thus made available for output. Word count jumpers (at present connected for 40 words per line) permit the

counter outputs to be applied to an 8-input NAND gate which, following completion of a data line, resets the sync disable flip-flop thus enabling the sync detectors, resetting the bit and word counters, and gating off the word sync output preventing the output of an extraneous word sync pulse generated by counter reset. This NAND gate has two inputs in addition to those from the word counter. These are from the bit counter, and delay the output of the NAND until 6 additional bits have been input following output of the last data word. Four of these are required to shift new data bits, following the last data word, into position in the first 4 bit positions of the shift register where possible sync detection could occur. (These bits will normally be 0101 gap filler code provided that the decoder is in sync with the incoming data.) The two additional bits are provided as a margin for error in the bit count (the Miller code system is not completely error free) without loss of sync.

If the data being decoded was recorded using the parity check mode the mode flip-flop will be set as described above. In this case a 1-level is supplied to the mode output of the decoder (used, via a lamp driver, to illuminate the partiy check indicator on the console control unit) and is also applied to gate on the parity checker (IC Type SN 74180) and to supply, via the NOR gate in the LSB output line, a zero data bit to replace the parity check bit present on this line at the output of the shift register. The parity checker is actually identical to the parity generator of Fig. 46 (paragraph 13), but is connected differently to perform the checking function, as shown in Fig. 50. Since the output of the parity checker is valid only when a data word is in proper position for output in the shift register it is necessary to strobe the output of the parity checker with the word sync pulse available at that time. Thus, the parity error output of the encoder is a 1-level pulse coincident with the word sync pulse if the corresponding data word contains a parity error, and is zero otherwise.

If the mode flip-flop is reset, indicating that the input data was recorded using the 8 data bit mode, a zero level is applied to the mode output and the parity checker is gated off. The least significant bit (LSB) from the shift register will now be a data bit and is permitted to pass to the data output via the NOR gate. Note, in this case, that this bit which has previously been inverted by the parallel input-serial output encoder (paragraph 13) is reinverted by the NOR gate and thus appears correctly at the decoder output.

If a decoder is not in use at a particular time (i.e., the corresponding video selector switch is set to other than a serial data position, or if the recorder is not in the REPRODUCE or RECORD mode (the RECORD mode also provides reproduction of the data immediately after recording), the corresponding parity error and mode indicators would be illuminated at random which would be distracting to the operator. To prevent this, a means for disabling the decoder under

these conditions has been provided. The four 2-input NAND gates of Fig. 50 perform this function from logic levels provided by the video selector switch and from the reproduce relay located in the recorder control unit (Fig. 28).

This system for disabling the decoder also permits sync to be established for recovery of the first data frame after turn on provided that this frame is preceded by gap filler code. (This condition is fulfilled by the parallel input-serial output encoder for the first data frame recorded after turn on - see paragraph 13, above.) Operation is as follows: If the decoder is disabled (recorder not in REPRODUCE -see above) the D input of the sync disable flip-flop will be zero (F) and this flip-flop will be reset either (1) by chance when power is first applied, (2) by receipt of a 4 digit sync code in random data from the free running Miller code system, or (3) by the decoder word counter and gate after clock pulses equivalent to one data line have been received. Since the Miller code output data clock free runs at approximately the correct rate whenever power is applied to the recorder (even though data is not being reproduced) reset will always occur within approximately 125 microseconds following encoder disable provided that recorder power is on. With the sync disable flip-flop reset, the sync detectors are enabled and the counters are reset and disabled. The system must now remain in this state until the encoder disable signal is removed since the sync disable flip-flop cannot again be set while this signal is present. After the encoder disable signal is removed (by placing the recorder in the REPRODUCE mode) the first sync code detected by the decoder will set the sync-disable flip flip and the decoder will continue to operate, in sync, as previously described.

Although beyond the scope of the present discussion it can be shown, and easily demonstrated experimentally, that synchronization of the serial data decoder with the incoming data will normally occur within a few data lines after turn on even if started at random (or after loss of sync due to tape drop out) rather than in the manner described above. The only requirement is that the data for successive data lines be at least somewhat random in nature, a condition practically certain to prevail in any normal imaging application.

17. Video Data Buffer

Since the parallel video data from the serial data decoders (par. 16) and also from the A/D converter (par. 12) are only available during a brief time interval, in order to display this data via the visual display channel, each data word must be stored in a buffer until the next word becomes available. This is the function of the video data buffer, Fig. 52. Two identical units are used, one for each visual display channel (see Fig. 21).

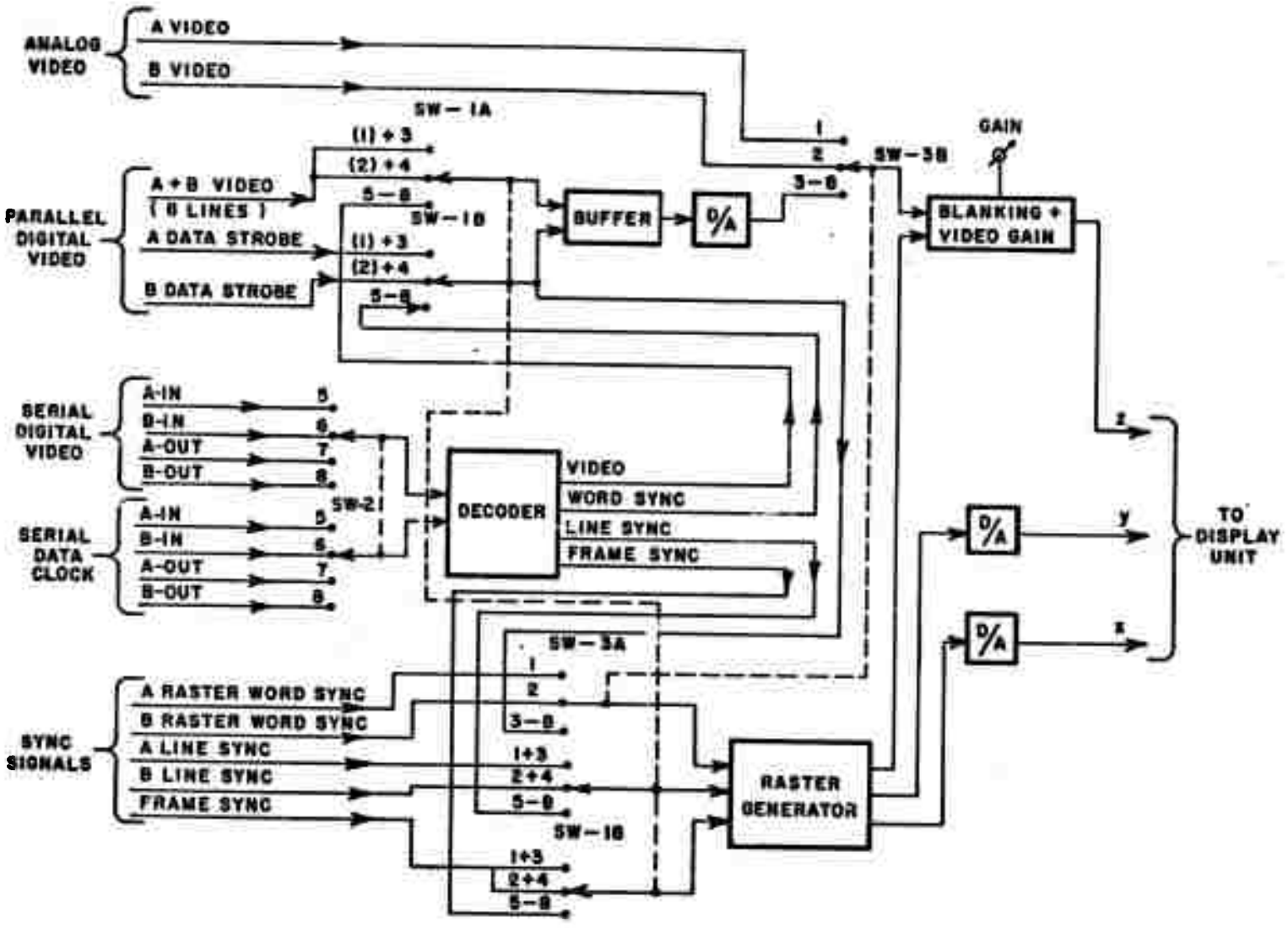
The SN 7450 AND-NOR gates (Fig. 52) and inverter 5 of the SN 7404 Hex inverter controlled by the serial data switch input provide a means for selecting data from either the serial decoder or the A/D converter for application to the buffer. Since the AND-NOR's invert the data, each bit is re-inverted by one of the remaining inverters (SN 7404) before input to the buffer. The buffer is a type SN 74100 8-bit bistable latch clocked via the digital data strobe input. (A suitable data strobe is provided via the video display switching unit -see paragraph 18, below.) The outputs of the latch follow the input data when the clock is high. When the clock goes low the data then present at the inputs are retained at the latch outputs until the clock again goes high to load the next data word.

18. Video Display Switching

Associated with each visual display channel is a versatile video display switching system by means of which either display unit may be used to display analog video (ANALOG), sampled and digitized video (PARALLEL), the serial digital data applied to the input of the recorder (SERIAL IN), or the output of the magnetic tape recorder (SERIAL OUT) for either Channel A or Channel B as desired. The desired signals for display are selected by means of the channel selector and video selector switches on the console control unit Because of the high frequency signals involved and the location of the various signals to be switched in diverse parts of the system, however, direct signal switching via the control unit switches is not feasible. Consequently, these switches only apply appropriate logic levels to 3 binary switching lines (1), (2), and (4) (see Fig. 21) which are then routed to various solid state IC switching devices (via additional logic, in some cases) located elsewhere in the system.

A block diagram of the overall video display switching system for one display indicator channel (the second channel is identical) is given in Fig. 19. In this diagram all solid state switching elements are shown as conventional switches and control inputs to the various devices are omitted to clearly indicate the functional arrangement of the signal paths. All switching elements are labeled for reference and all which bear the same number (example: SW-1A and SW1-B) operate together as a multi-pole switch although those bearing a different subscript (i.e., SW-1A and SW-1B) are physically separate units which are mounted on different circuit boards. The various possible positions of these switches are numbered in Fig. 19, and these numbers (which are the numerical values of the corresponding digital switching lines for the corresponding positions) correspond to settings of the channel and video selector switches as indicated at the bottom of the figure.

Actual locations of the switching elements of Fig. 19 are given in Table VIII while the logic input levels applied to the switching elements for the various possible setting of the channel and video selector switches are given in Table IX.



SWITCH POSITIONS

1. A—ANALOG	4. B—PARALLEL	7. A—SERIAL OUT
2. B—ANALOG	5. A—SERIAL IN	8. B—SERIAL OUT
3. A—PARALLEL	6. B—SERIAL IN	

Fig. 19. Video display switching block diagram.

TABLE VIII
VIDEO SWITCHING ELEMENT LOCATION

Switching Element	Circuit Board
SW-1A	Video Data Buffer
SW-1B	Video Display Switching Unit
SW-2	Serial Data Decoder
SW-3A	Video Display Switching Unit
SW-3B	Video Switching and D/A Converter

One circuit board (per channel), the video display switching unit, is associated exclusively with the video switching system and will now be described with reference to the logic diagram, Fig. 53.

The 1st data selector and one half of the 2nd data selector (IC Type SN 74153) perform the function of SW-1B (Fig. 19). The binary inputs A (1) and B (2) are driven from the (1) and (4) switching lines, respectively, so that input values for the various positions of the channel and video selector switches are as given in Table IX. The second half of the 2nd data selector provides logic voltages to operate SW-1A located on the video data buffer circuit board.

One half of the 3rd data selector performs the function of SW-3A (Fig. 19), while the other half is spare. The required inputs for this switch are slightly more complex, as seen from Table IX and to obtain these inputs the A (1) input is driven from the (1) switching line while the B (2) input is driven by the (2) or (4) switching lines via the lower NOR gate and inverter of Fig. 53.

Switch SW-3B (Fig. 19) is a solid state analog switching device which requires a 1-level (true) signal applied to the selected input line while a 0-level (false) is applied to the remaining input lines. The required signals (see Table IX) are derived from the input switching line logic levels via the NOR gate, AND gates, and inverters as shown in Fig. 53.

19. Raster Generator

The raster generator produces, from word, line, and frame sync inputs, the digital binary output signals required to drive the x and y axis inputs of the display indicator via digital-to-analog converters. Three identical units are used, one for each display indicator. The associated D/A converters which convert the digital outputs to staircase raster waveforms are mounted on the video switching and D/A converter circuit board described in paragraph 20, below. A logic diagram for the raster generator is given in Fig. 54, and the corresponding timing diagram in Fig. 55.

TABLE IX
VIDEO SWITCHING INPUT LEVELS

Video Switch Positions		Input Switching Lines			Data Selector Inputs						Analog Switch	
					SW-1		SW-2		SW-3A		SW-3B	
Chan.	Selector	(4)	(2)	(1)	(B)	(A)	(B)	(A)	(B)	(A)	Switch	Line true
A	Analog	0	0	0	0	0	0	0	0	0	1	
B	Analog	0	0	1	0	1	0	1	0	1	2	
A	Parallel	0	1	0	0	0	1	0	1	0	3	
B	Parallel	0	1	1	0	1	1	1	1	1	3	
A	Serial In	1	0	0	1	0	0	0	1	0	3	
B	Serial In	1	0	1	1	1	0	1	1	1	3	
A	Serial Out	1	1	0	1	0	1	0	1	0	3	
B	Serial Out	1	1	1	1	1	1	1	1	1	3	

The vertical raster generator is basically a binary counter driven by the raster word sync input with reset via line sync or an end-of-line gate. Since it is the faster of the two generators in this system (i.e., the raster consists of 40 vertical lines, each composed of 40 individual sample points, or words, see Fig. 14) it also contains circuitry for unblanking the beam (z-axis intensity) for each data word. Operation is as follows (see Figs. 54 and 55).

Arrival of a line sync pulse will reset the vertical raster counters to zero if not already reset via the end-of-line gate following a previous line. This is the required output for the 1st word of each raster line (see Fig. 55, sheet 1). Each raster word sync pulse which now arrives (coincident with the beginning of a data word cell) triggers the unblanking gate 1-shot. The trailing edge of the word sync pulse is used to insure that data (from the serial decoder and buffer) is actually available at that time. The output of the unblanking gate 1-shot is then fed to the blanking input of the video switching and D/A converter (paragraph 20) where it is applied to unblank the CRT beam for display of each data word. The trailing edge of the unblanking gate 1-shot output is then applied, following a small delay obtained via the raster step delay 1-shot, to increment the vertical raster counter, thus moving the (now blanked) CRT beam into position for the next data word.

The raster step delay is not included in the timing diagrams of Fig. 55 since its function is not directly associated with raster generator operation. It is required because, in general, the propagation delay of the z-axis channel is greater than that of the x and y axis channels because of the switching, blanking, and amplifier circuits contained in the video switching and A/D converter (see par. 20, below) and perhaps also in the display indicator as well. Hence this delay, which may be adjusted as required for a given visual display indicator, provides a means for delaying the y-axis raster steps so that they arrive at the indicator CRT while the beam is blanked as shown in Fig. 55.

After the last word of the line (40th word in the present system - corresponding to a vertical raster output count of 39) has thus been displayed the counter is incremented once more, but is then immediately reset via the end-of-line gate in preparation for the next raster line. This arrangement gives the maximum amount of fly-back time possible and hence relieves the frequency response requirements of the display indicator and settling time requirement of the associated D/A converter. In the event that a word sync pulse is missed, however, or that the raster generator is not properly synced with the incoming signals, the raster counters are later reset via the line snyc pulse so that proper sync is re-established for the next raster line.

Raster lines are interlaced horizontally as previously mentioned in Chapter III-B-3 (see Fig. 14), hence the horizontal raster generator is somewhat more complex. It consists basically of a type SN 74193 4-stage synchronous up-down binary counter with 2 additional stages (consisting of an SN 74107 dual flip-flop) driven by the line sync input pulses, reset by the frame sync input, and with appropriate gating to produce

the following count sequence: (0, 2, 4, 6, ... 38, 39, 37, 35 ... 5, 3, 1). Operation is now described with reference to the logic diagram (Fig. 54) and timing diagrams (Fig. 55, sheets 2 and 3).

For discussion of all previous circuits the point of reference in time (datum line on the timing diagrams) has been conveniently taken as the midpoint of the dead space between data lines. In this frame of reference, line sync precedes frame sync (when present) which in turn precedes the 1st data word of each line. However, for a system in continuous operation this reference point is arbitrary, and for discussion of the horizontal raster generator a reference point (datum line) immediately preceding the frame sync pulse is more convenient. With respect to this frame of reference, frame sync first occurs (see Fig. 55, sheets 2 and 3) followed by the word sync pulses for the first data line (not shown on these diagrams), and finally, the 1st line sync pulse which now occurs at the end of the line rather than at the beginning, and so on for the remaining lines of the frame.

When the frame sync pulse arrives the raster counter (SN 74193 and SN 74107) is reset to zero for the 1st raster line. The up-count NAND is now enabled via the $\overline{Q}$ output of the "1" counter (SN 74107) and line count NAND, while the down count NAND is disabled via the Q output of the "1" counter and the zero count NAND. Thus when the first line sync pulse occurs (after the 1st data line) the counter is incremented. Note that the first stage of the counter produces the "2" output (while the "1" output is obtained from a special counter stage). Thus the counter counts by 2's as required for the interlaced scan. After the first line sync pulse is received, the output of the zero count NAND goes high; however the down count NAND is still disabled by the "1" counter so that counter gating remains as before. Thus the counter continues to increment (by 2's) with each line sync pulse until the count of 38 is reached. Note that the 5th stage of the counter, although composed of an SN 74107 flip-flop, is wired to operate exactly as the previous stages (SN 74193).

At this point, the output of the line count NAND goes low gating off the up-count NAND and gating on the clock input to the "1" counter. Hence on arrival of the next line sync pulse the "1" counter is set producing an output count of 39. The outputs of the "1" counter are also applied to enable the down count NAND and disable the up count NAND. Note that while the clock input to the "1" counter remains enabled, this counter will not reset on the next line sync pulse because the levels applied to the J and K inputs only permit this counter to be set via the clock input.

The next line sync pulse will then cause the counter to decrement (by 2) producing the output count of 37. At this point the line count NAND goes high but this has no immediate effect on counter operation (since the up-count NAND remains gated off via the "1" counter and the presence or absence of clock pulses to the "1" counter can have no further effect until this counter has again been reset via a frame sync pulse). Thus the counter continues to decrement (by 2's) until the count of 1 is reached for the last raster line of the frame.

At this point the output of the main counter (1st 5 stages) is zero (i.e., the only non-zero output is provided by the special "1" counter flip-flop). The main counter outputs are then applied to the zero-count NAND (via the NOR gates from the 1st 4 stages and a direct connection from the 5th stage) to produce a low output which is applied to disable the down-count NAND. Thus the last line sync pulse received after the last data line is gated off and has no effect. If this were not done, the last line sync pulse would recycle the counter backward to maximum output producing an undesired glitch which, although blanked on the CRT screen, would put undue demands on the D/A converter and display indicator response time required to correctly display the 1st data point of the following line.

The cycle is now complete and arrival of the next frame sync pulse will reset the "1" counter flip-flop to produce a zero-count for the 1st line of the next frame. As mentioned previously, the frame sync pulse is also applied to all other horizontal raster counter stages so that if the raster generator has for any reason lost sync with the incoming data, proper sync will be re-established at this point.

20. Video Switching and D/A Converters

The video switching and D/A converter PC board contains digital-to-analog converters for use with the x and y axis inputs from the raster generator (par. 19, above), a z-axis D/A converter used during display of digital video signals, a 4-section digitally-controlled analog switch for video switching and blanking together with level converters for driving this switch, and a video summing amplifier for combining the desired video signal with the blanking signal. Three outputs are provided to directly drive the x, y, and z axis inputs of the visual display indicator.

Two identical units are used for driving the two console display indicators and a third unit is used for analog displays only for the scanner-mounted display indicator. This unit is identical except that it does not contain the z-axis D/A converter (not needed for analog video display) and has different values of x and y axis D/A converter load resistors and a different value of video amplifier feed back resistor because of the differing input sensitivities of the associated display indicator. Circuit operation is described with reference to the logic diagram, Fig. 56.

Inputs for the x and y axis D/A converters are supplied from the raster generator as shown in Fig. 21 (or Fig. 20, for the scanner-mounted unit). They convert the digital raster signals into analog staircase deflection voltages required by the visual display indicator. These D/A converters are 8-bit units (allowing for possible future increase in image resolution) although only the six most significant input bits are presently used for each unit to generate the present 40 x 40 element display. The x and y axis circuits are identical except for differing values of load resistors (for the console units) required to accommodate the differing x and y input sensitivities of the display indicator.

The z-axis D/A converter is electrically identical to those described above except for the value of load resistor (chosen to yield a ±1 volt peak-to-peak output to match that of the analog video signals). Input is supplied from the video data buffer as shown in Fig. 21. All 8 input data bits are used. The video output is applied to the z-axis channel, when one of the digital video signals is selected for viewing (see paragraph 18, above), via the analog switch as described below.

Three sections of the analog switch (IC Type CD 4016D) are used for selecting the desired video signal: Channel A analog, Channel B analog, or the output of the z-axis D/A converter, for application to the video amplifier. The desired section of the switch is turned on by applying a +5 volt level to the associated control input while the remaining switches are turned off via a -5 volt control input. The selected signal is then applied to the video amplifier via the associated summing input resistor while the other two video signal inputs are effectively disconnected.

The 4th section of the analog switch (switch D) is used for unbanking the CRT beam (which is otherwise biased beyond cut off) during display of an image element. The blanking input from the raster generator (which is 0-logic level during a data word, and 1-level otherwise) is first applied to the blanking amplifier which inverts the signal and provides output levels (+5 v or -5 v nominal) required by the analog switch. This amplifier is a high frequency operational amplifier operated in the comparator mode (i.e., no feedback resistor) for fast switching between the two output levels. When the switch is turned on, by a +5 volt signal from the amplifier, +5 volts (from a low impedance source for fast rise time) is applied via the switch to the video amplifier input via the associated input summing resistor to unblank the CRT beam. When this signal is not present the beam is kept blanked by means of the bias applied to the video amplifier input from the -5 volt source and associated input summing resistor.

Since the analog switch is a bipolar device which cannot be controlled directly via the standard TTL logic levels, level converters are required on the three input video switching lines. These are provided by the triple operational amplifier type CA 3060. Each section is identical, and operates as a non-inverting comparator producing a +5 volt (nominal) output to turn on the corresponding analog switch when the input level is high (true) and a -5 volt output level when the input is low (false).

21. Video Level and Error Indicators

The video level and error indicator board shown in Fig. 57 contains logic circuits to sense a full scale reading for video level from the A/D converter for either A or B channel, and to provide an output pulse, for each such occurrence, of sufficient width to be visible on the video level indicator for the corresponding channel. This board also contains circuits to lengthen any parity error pulses received from the serial data

decoder parity error checkers for the two display channels (see par. 16) to a length suitable for visual display. Buffer drivers are included on this board to directly drive the associated 24 v video level and parity error indicator lamps.

Parallel digital video data from the A/D converter (Channel A and B video data are multiplexed - see par. 12) are applied to the inputs of an 8-input NAND gate (SN 7430) which produces a low output level whenever a full scale input (i.e., all 1's) occurs. This output is first inverted and then applied to one input of each of two NAND gates (SN 7400) used to demultiplex the resultant signals to the appropriate channel. The other input for each of these NAND gates is supplied by a 1-shot (SN 74123) for delay, driven by the trailing edge of the data strobe for the corresponding video channel. Thus an output pulse, coincident with the delayed data strobe, appears at the output of the NAND gate for either A or B channel whenever a full scale signal level appears for that channel at the parallel data input. The output of each demultiplexer NAND gate is then applied to trigger another 1-shot (SN 74123) which generates a pulse of sufficient width (approx. 30 ms) to be individually visible on the corresponding video level indicator. Each indicator lamp is driven by two parallel sections of the buffer driver (SN 7407) which grounds one side of the lamp (the other side is connected to the +24 v supply) causing it to light for the duration of the output pulse.

Circuits similar to the output pulse 1-shots and lamp drivers above are used for each parity error channel. These 1-shots are triggered directly by the parity error pulses from the corresponding serial data decoder error checker. Since by nature of the Miller code system parity errors usually occur in bursts (due to tape drop out, dust flecks, etc.) rather than as single errors, the 1-shots for this application have a shorter pulse width (approx. 3 ms) which has been experimentally determined to yield a more useful measure of the intensity of error bursts likely to occur than do the wider pulses employed above.

All 1-shots used in these circuits are of the retriggerable type, hence if the output pulses exceed the cycle rate for the 1-shots, the corresponding indicator lamp will be continuously illuminated.

22. Voltage Dividers

There are numerous dc power supplies used throughout the system and it is desired to have panel indicators to signify proper operation of these supplies. The function of the voltage divider PC board is to provide for each of these various voltage sources, corresponding output logic levels suitable for application to standard TTL buffer-drivers to light the corresponding indicator lamps. A schematic diagram for these circuits is given in Fig. 58.

Circuits for all negative input voltages (except -1250 volts) are identical except for the values of the input resistors which are chosen consistent with the magnitude of each input voltage. Each circuit consists of a transistor inverter which, in the absence of the input voltage, is biased to saturation via the 1 K resistor and 3 series diodes thus producing a low logic output level. When the voltage is applied the transistor is cut off and a high logic output level is produced. A series diode is used in each base circuit to protect the associated transistor from any excessive applied inverse voltage.

Since -1250 volts cannot safely be applied to the card cage, a remote voltage divider (see Fig. 22) is used. The output of this voltage divider (≈150 mv) is then applied to the input of the (-1250 v) inverter circuit. Since this power supply and voltage divider can only supply a limited current (≈100 μ Amp) to the inverter circuit the parallel path to ground (3 series diodes) has been eliminated, a more sensitive transistor is used, and biasing and output divider resistors have been chosen accordingly. Otherwise, operation is the same as above.

Voltage dividers for the positive supply voltages are simple resistive dividers with resistance values appropriately chosen according to the supply voltage input. A value of 390Ω is used as the output resistance value for all dividers. The maximum value for this resistor is determined by the permissible voltage drop due to sinking current from the IC lamp drivers at low logic levels.

23. Lamp Drivers

The lamp drivers, Fig. 59, accept input logic levels (high = on, low = off) from the voltage divider board (par. 22) or from other TTL logic sources (i.e., the mode outputs of the serial data decoders) and provide switching to control the 24 volt indicator lamps. Either two or three sections are paralleled for each application via the jumpers (Fig. 59) depending upon the number of lamps to be driven (either 1 or 2 for this system) and upon the current ratings of the drivers (the type SN 7406 drivers used in the console have a higher current rating than the type SN 5406 drivers used in the scanner control unit).

The +24 v supply is connected to one side of each indicator lamp and the other side is connected to the corresponding lamp driver output. When a high level is applied to the driver input the output is effectively grounded, thus lighting the lamp.

V. SUMMARY

A dual channel, 200 frames per second, 10.6 micron infrared scanner, recorder, and visual display system developed and constructed for use in atmospheric imaging and image restoration experiments has been fully documented in this report. A general description, specifications, installation and operating procedures, and detailed theory of operation are given together with photographs, block diagrams, and complete schematics and timing diagrams.

Since this report was begun, the complete system has been delivered to the RADC Verona PATS test site and, using temporary primary optics (the telescope for which the scanner was designed was temporarily not available), preliminary tests were performed. No problems were encountered, and proper system operation was obtained without difficulty. The laser transmitting system is now being prepared, after which data recording for the imaging experiments[1] will be performed.

The recorded data will then be returned to the OSU ElectroScience Laboratory for processing. A playback and display system interfaced with the ESL DC 6024 data processing system is currently being constructed for this purpose. This system, as well as the data processing and experimental results obtained will be discussed in future technical reports.

APPENDIX I - SCHEMATIC AND TIMING DIAGRAMS

All schematic, logic, and timing diagrams for the system are collected in this appendix for easy reference. Details of circuit operation for the various circuits are given in Chapter IV which should be consulted for additional information.

Where possible, input signals for a given diagram enter on the left and output signals exit on the right for ease in following the circuit logic. All input and output connections to logic cards are indicated on the drawings by circles enclosing the corresponding card cage or edge connector pin numbers. Two types of card edge connectors are used for some circuit cards. These are the standard card cage edge connector (rear edge connector) which is always implied unless otherwise noted, and a special edge connector (front edge connector) which is bolted to the opposite edge of some circuit cards. These front edge connectors are used primarily for coaxial cable input or output connections to the circuit cards and are always labelled "front edge connector" when they appear on the logic diagrams.

Nearly all circuit logic elements are standard TTL integrated circuits. Details for the individual IC's may be found in the manufacturers literature.[10-13]

Many of the timing diagrams have a time reference line (datum line) which is usually taken to be the center of the dead space between successive data lines. One exception is the horizontal raster generator where a point in time just preceding the frame sync pulse is used (see Chap. IV, par. 19). Since successive data lines differ in length (although the time from the center of one dead space to the next is a fixed constant) an average length data line is normally used in the timing diagrams unless otherwise stated.

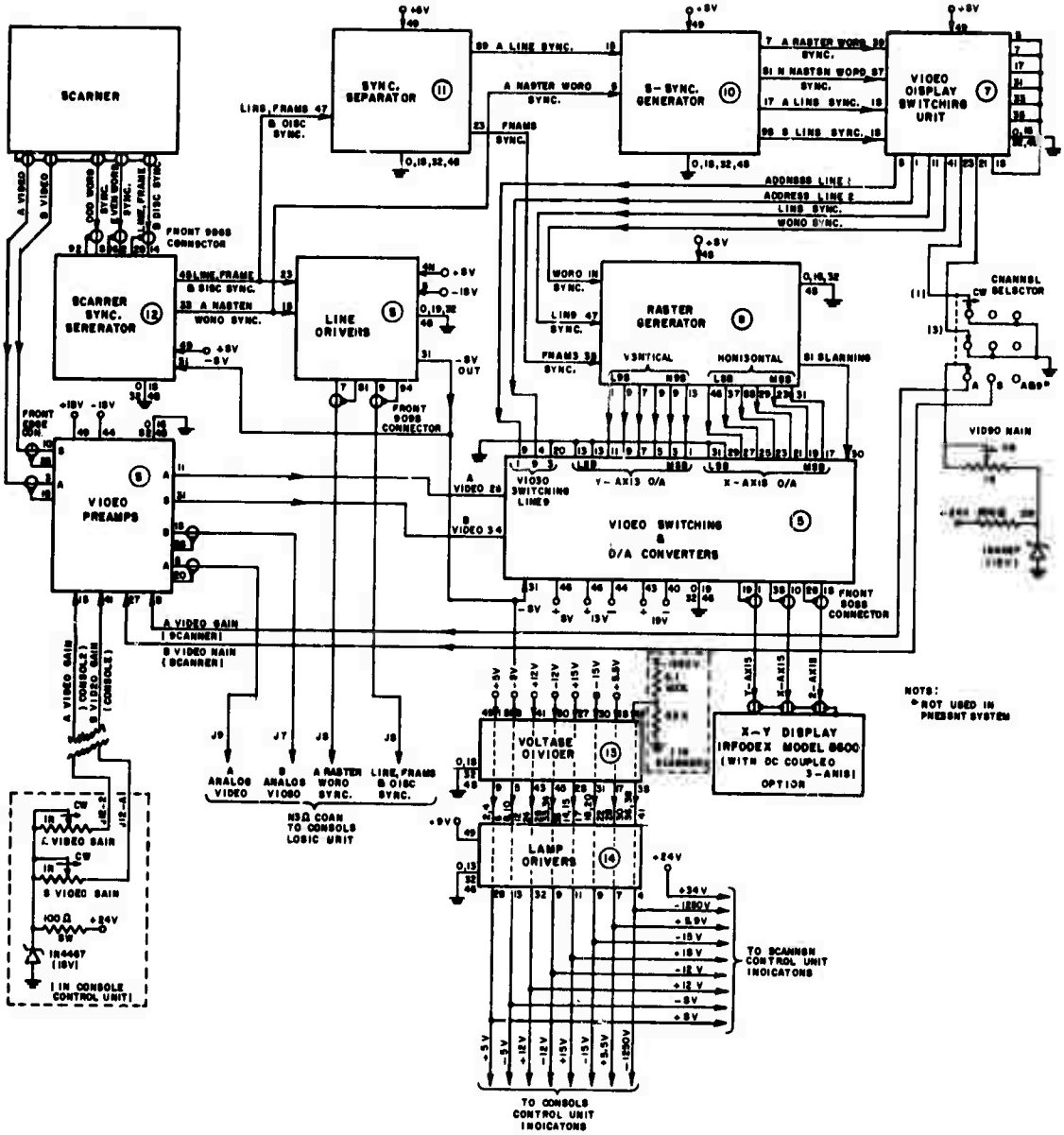


Fig. 20. Logic wiring diagram for telescope-mounted package.

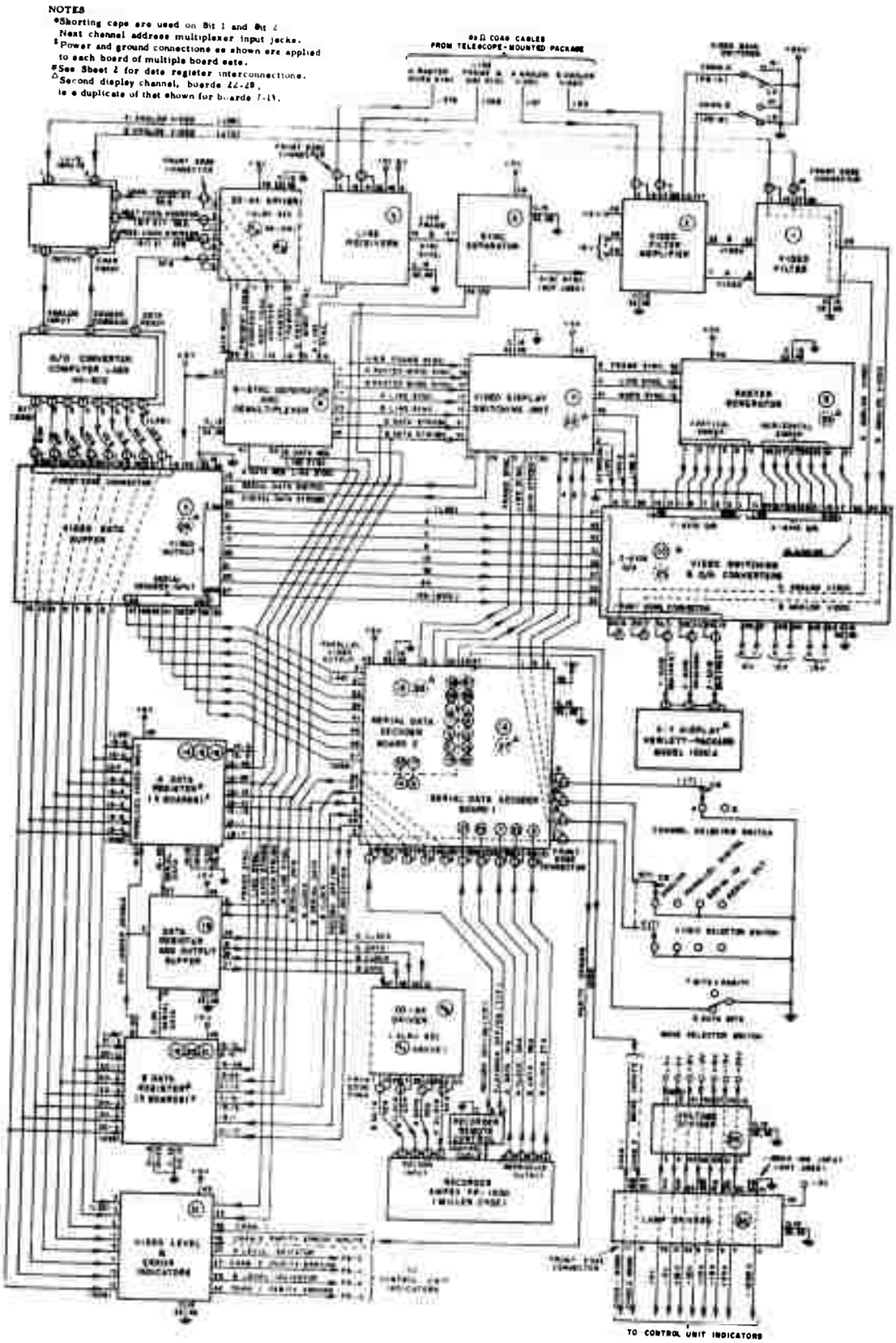
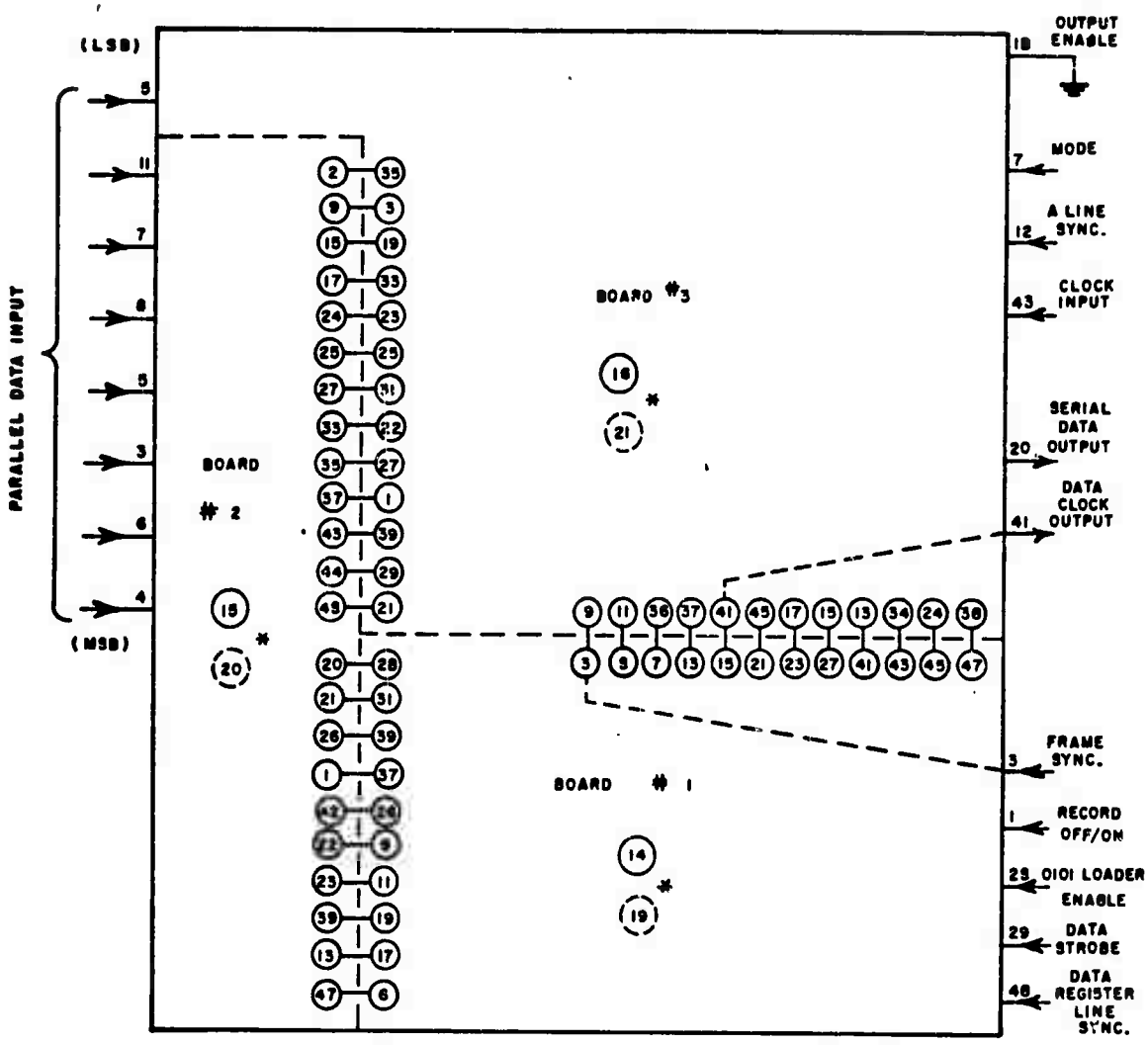


Fig. 21. Logic wiring diagram for system control package. Sheet 1 - Console logic.



*NOTE:
Slot numbers for Channel A are enclosed by solid circles.
Slot numbers for Channel B are enclosed by dashed circles.

Fig. 21. Logic wiring diagram for system control package. (cont.)
Sheet 2 - A and B data register interconncections.

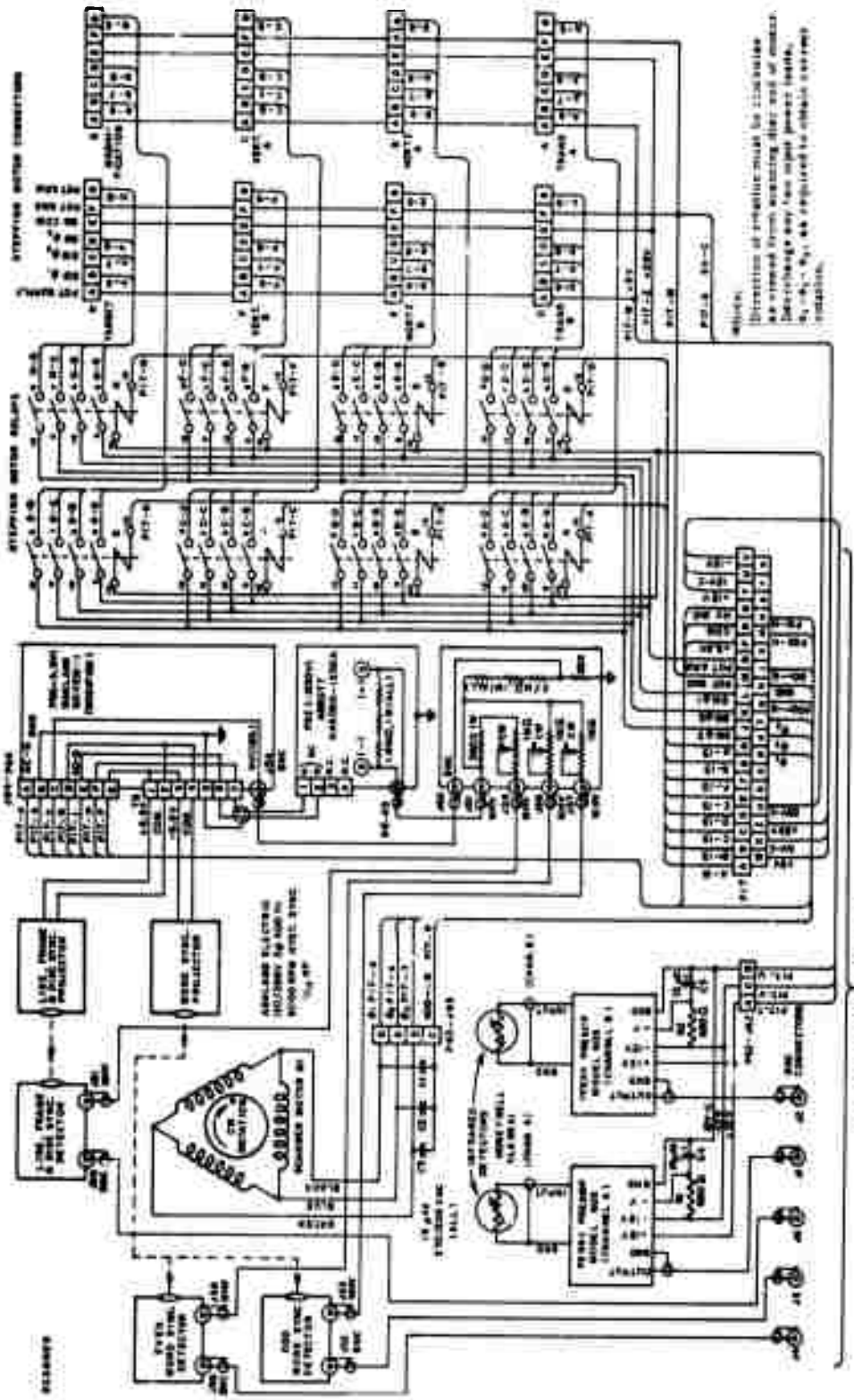


Fig. 22. Scanner wiring diagram.

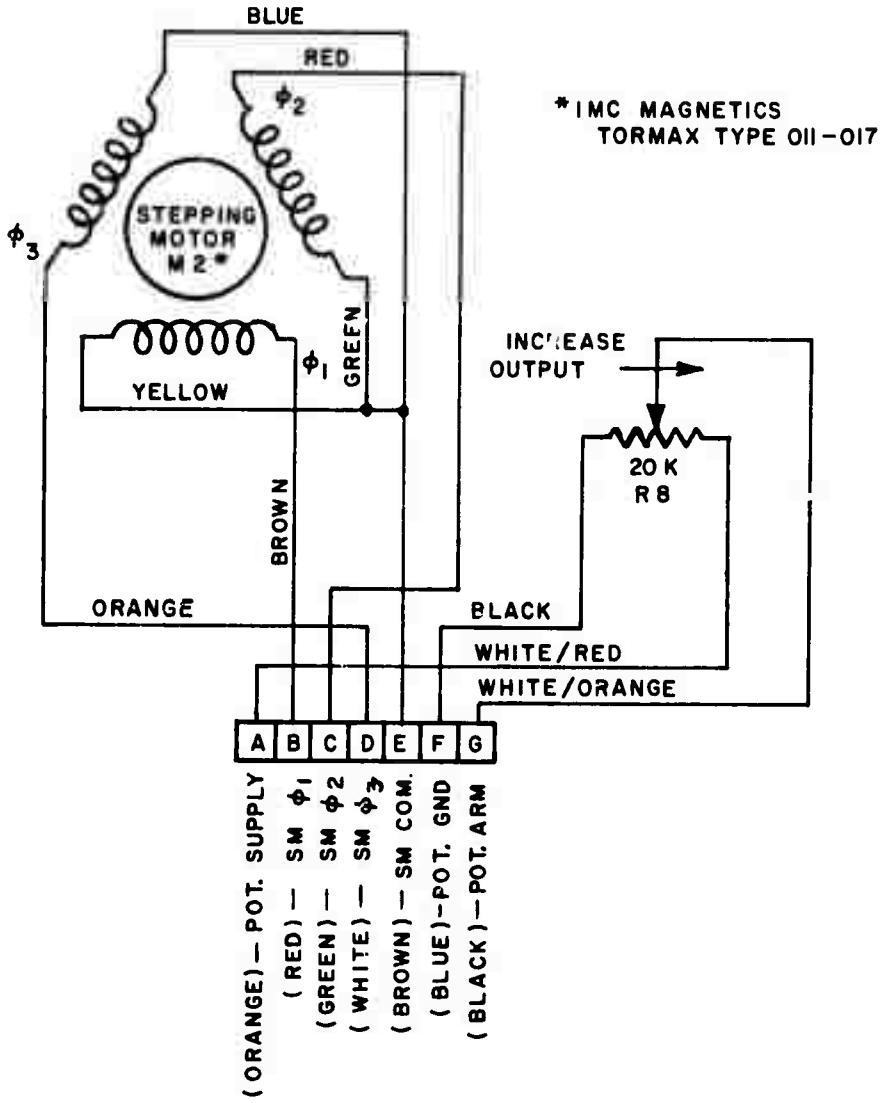


Fig. 23. Stepping motor and position pot. wiring diagram.

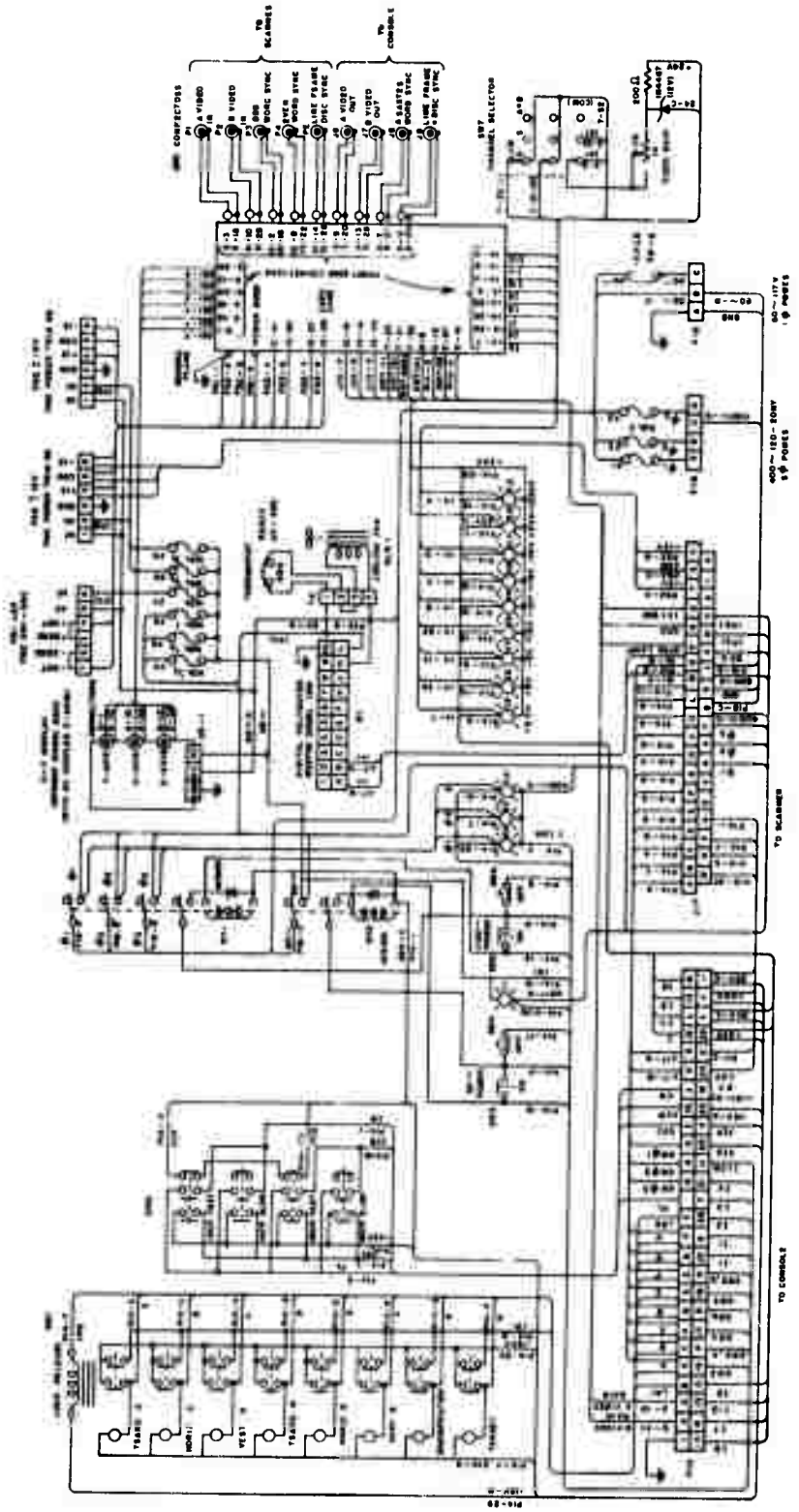


Fig. 24. Scanner control unit CU-2 wiring diagram.

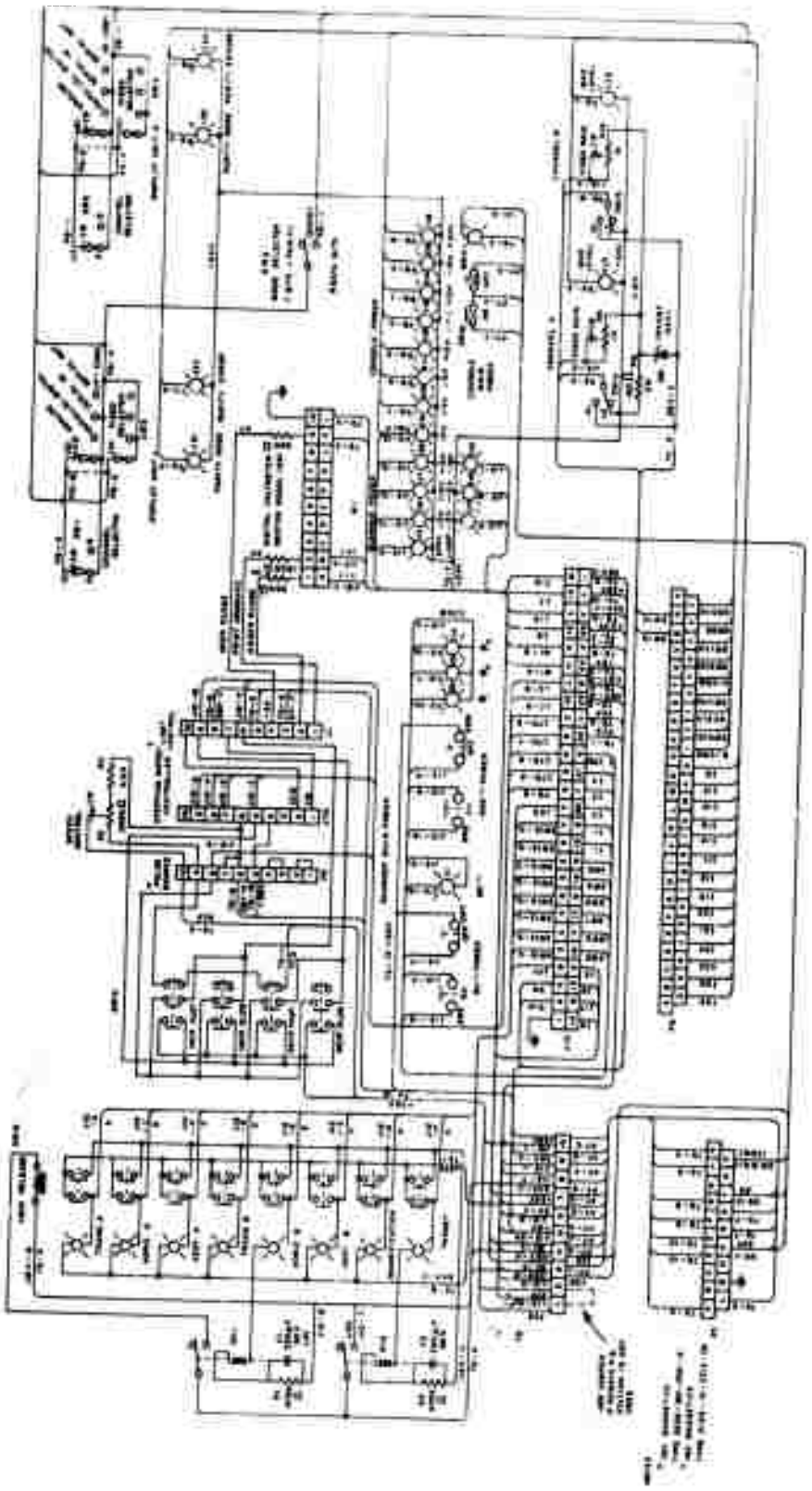


Fig. 25. Console control unit CU-1 wiring diagram.

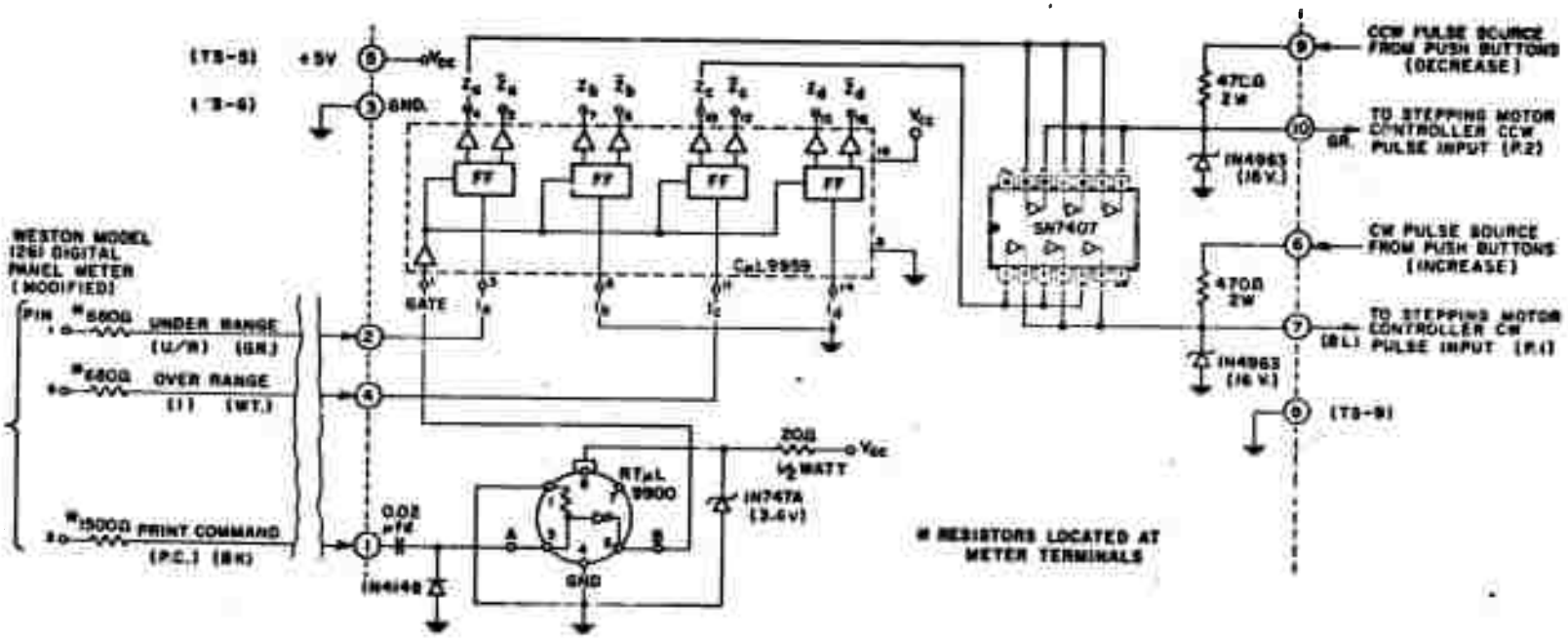


Fig. 26. Stepping motor limit control schematic diagram.

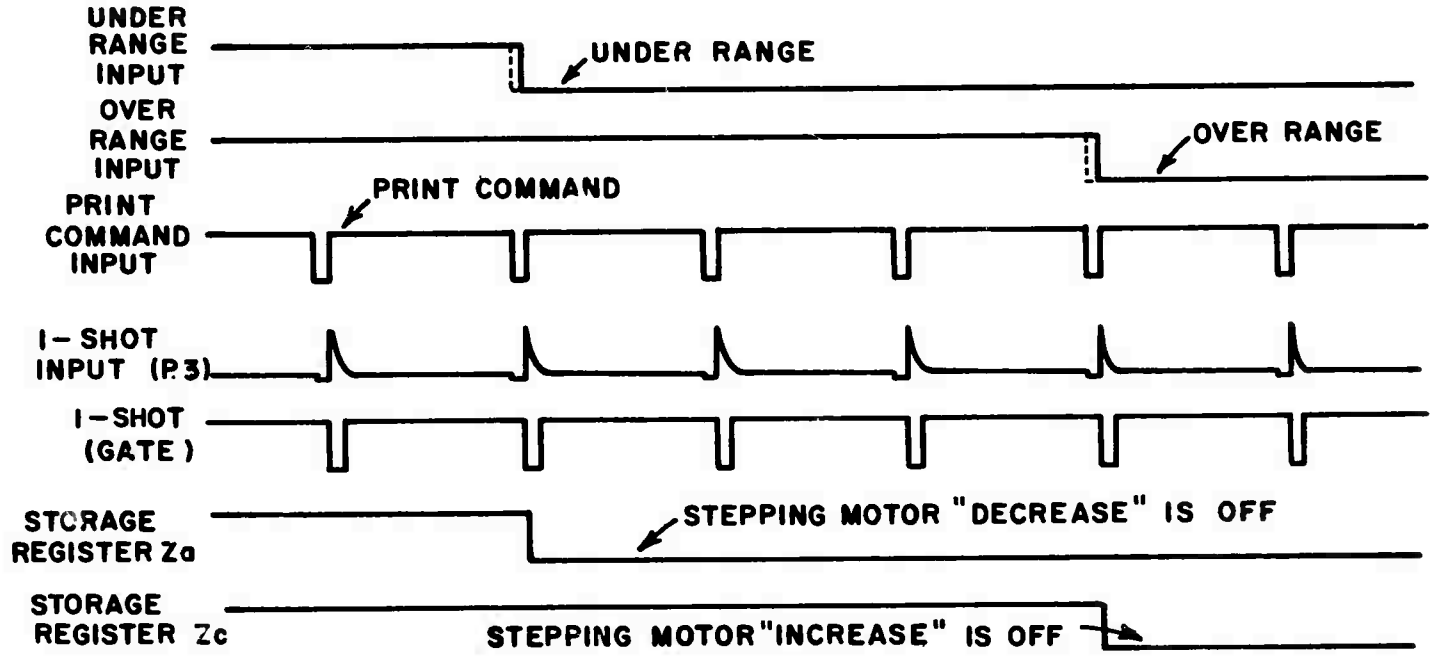


Fig. 27. Stepping motor limit control timing diagram.

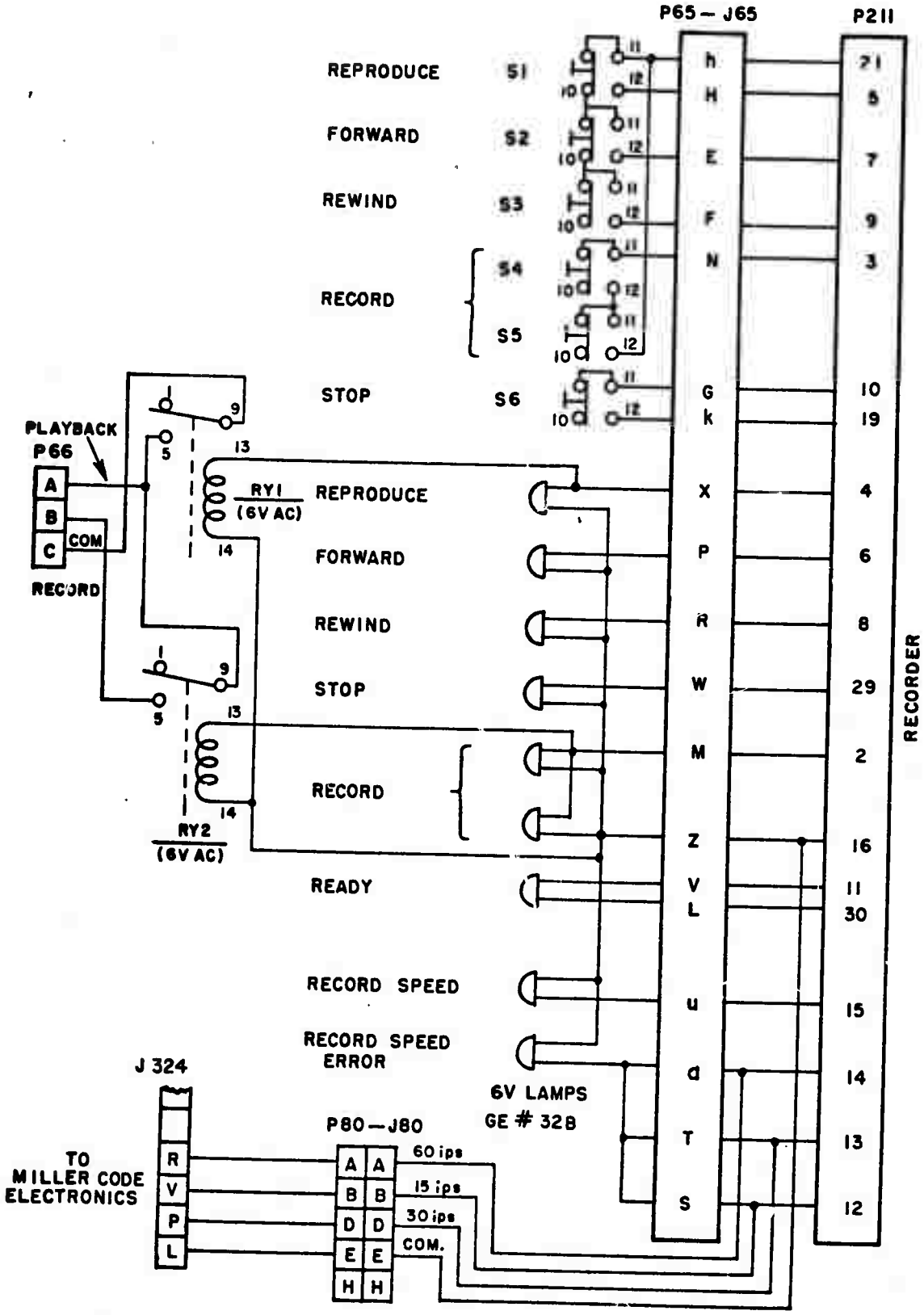


Fig. 28. Recorder control unit RCU-1 wiring diagram.

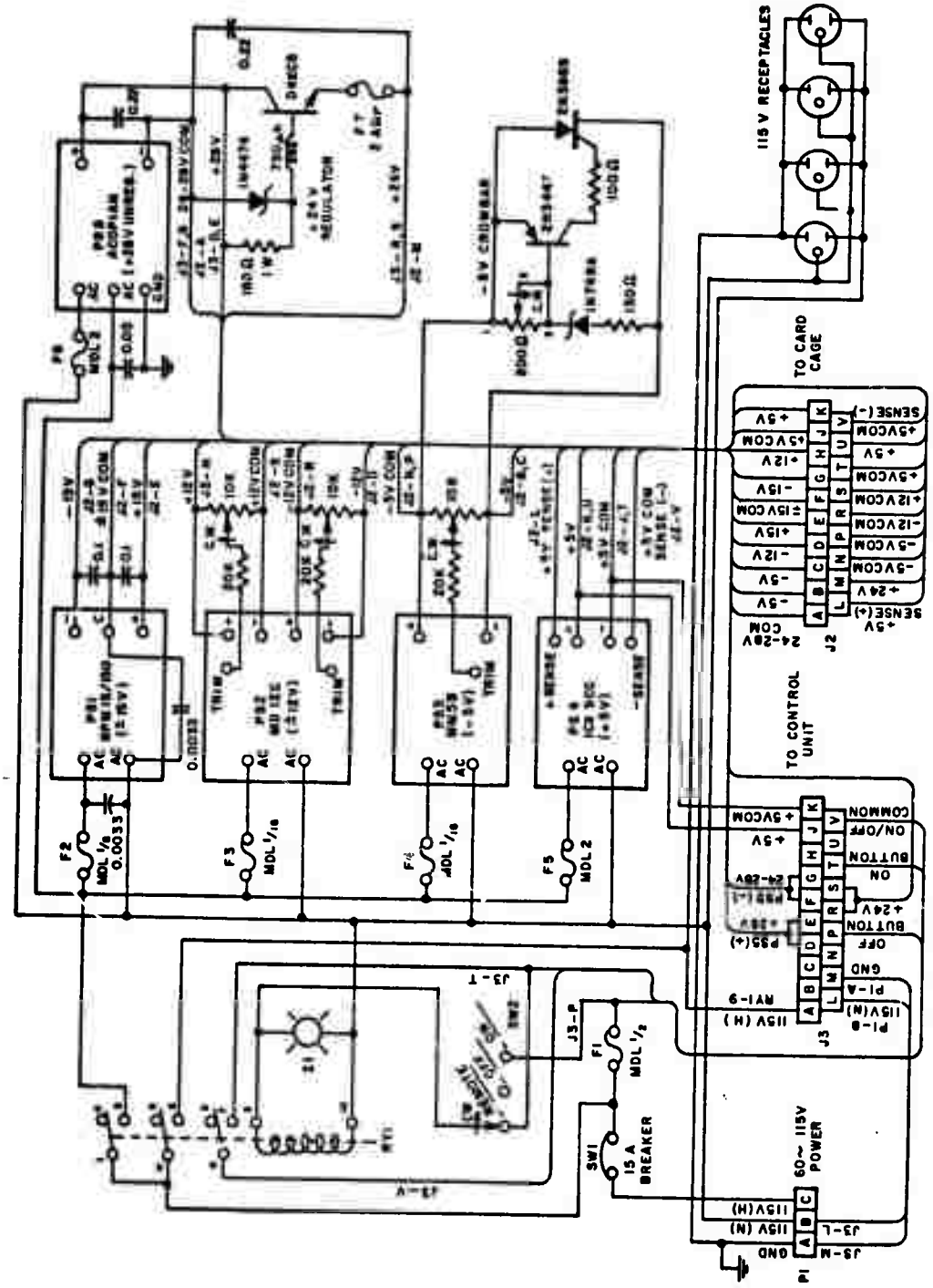


Fig. 29. Logic power supply LPS-1 wiring diagram.

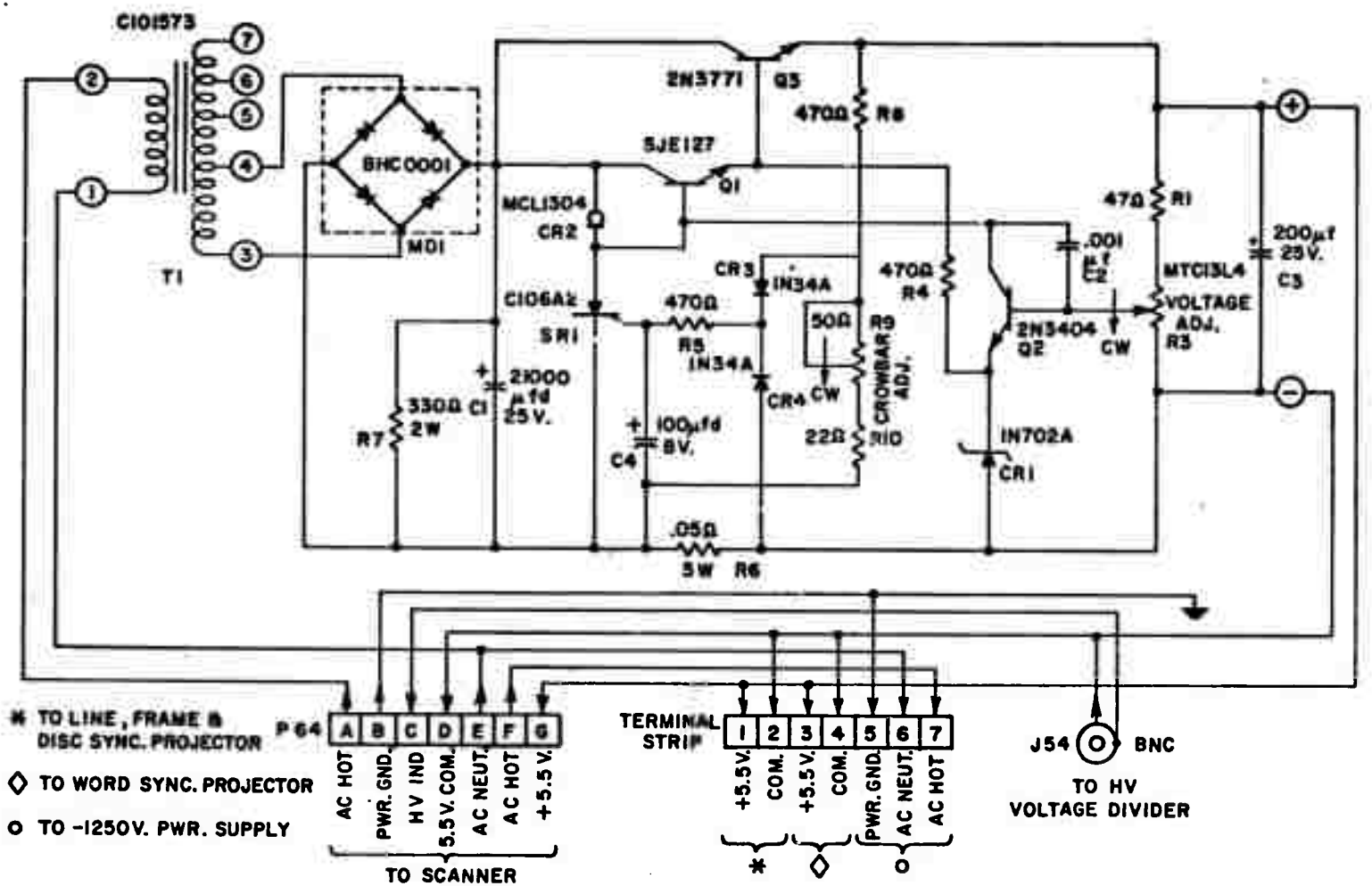


Fig. 30. +5.5 volt power supply schematic diagram.

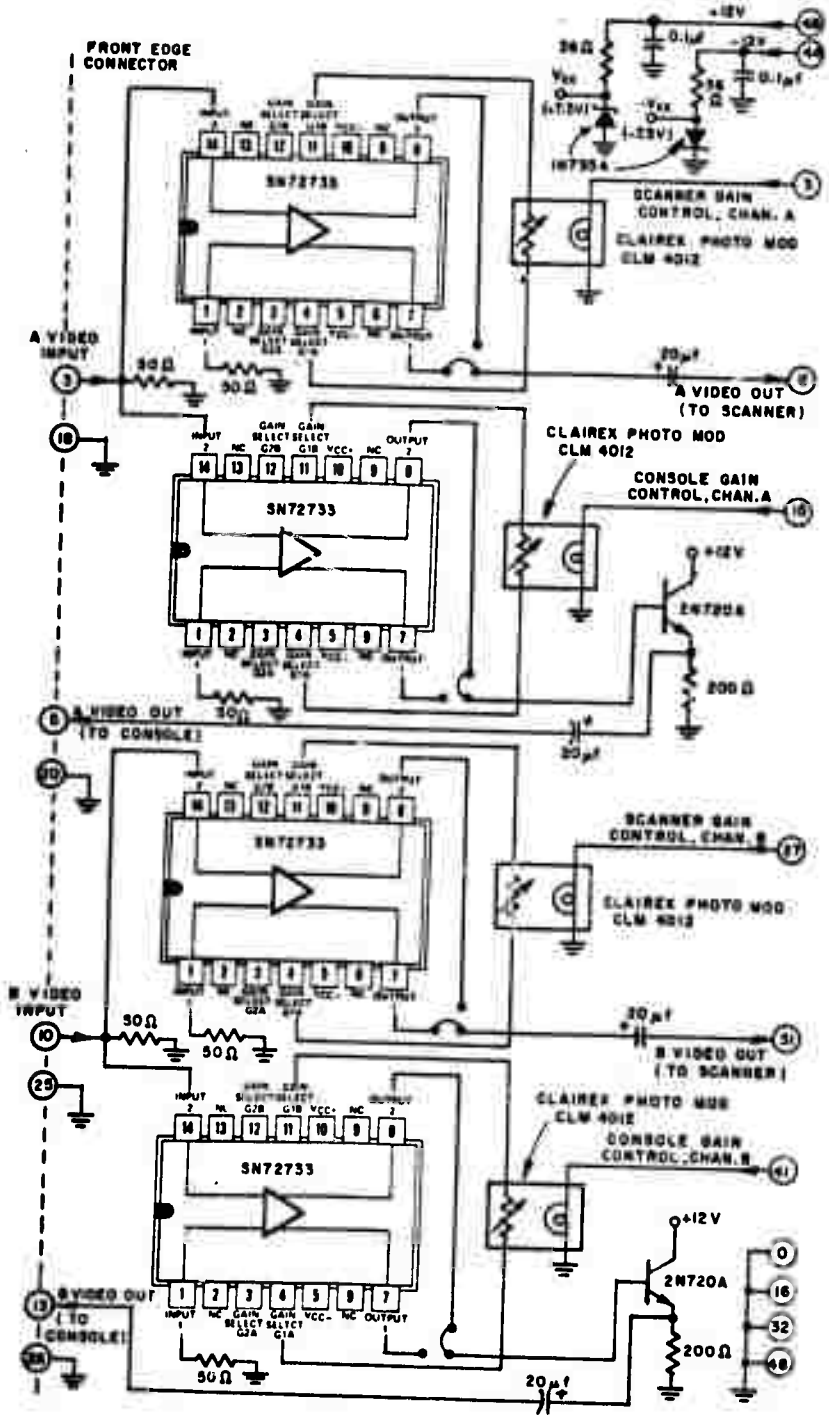


Fig. 31. Video preamps schematic diagram.

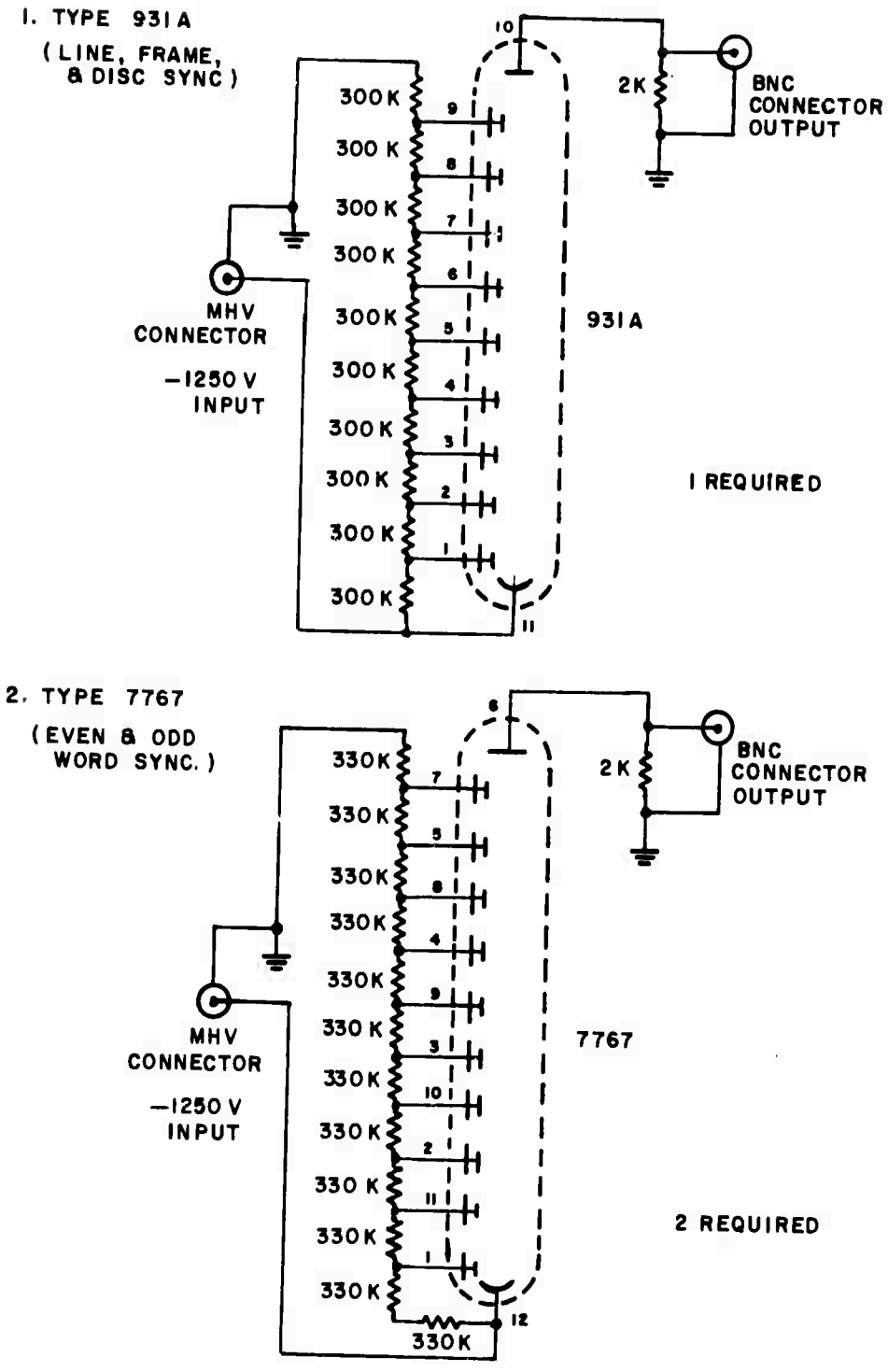


Fig. 32. Sync detector photomultiplier circuits.

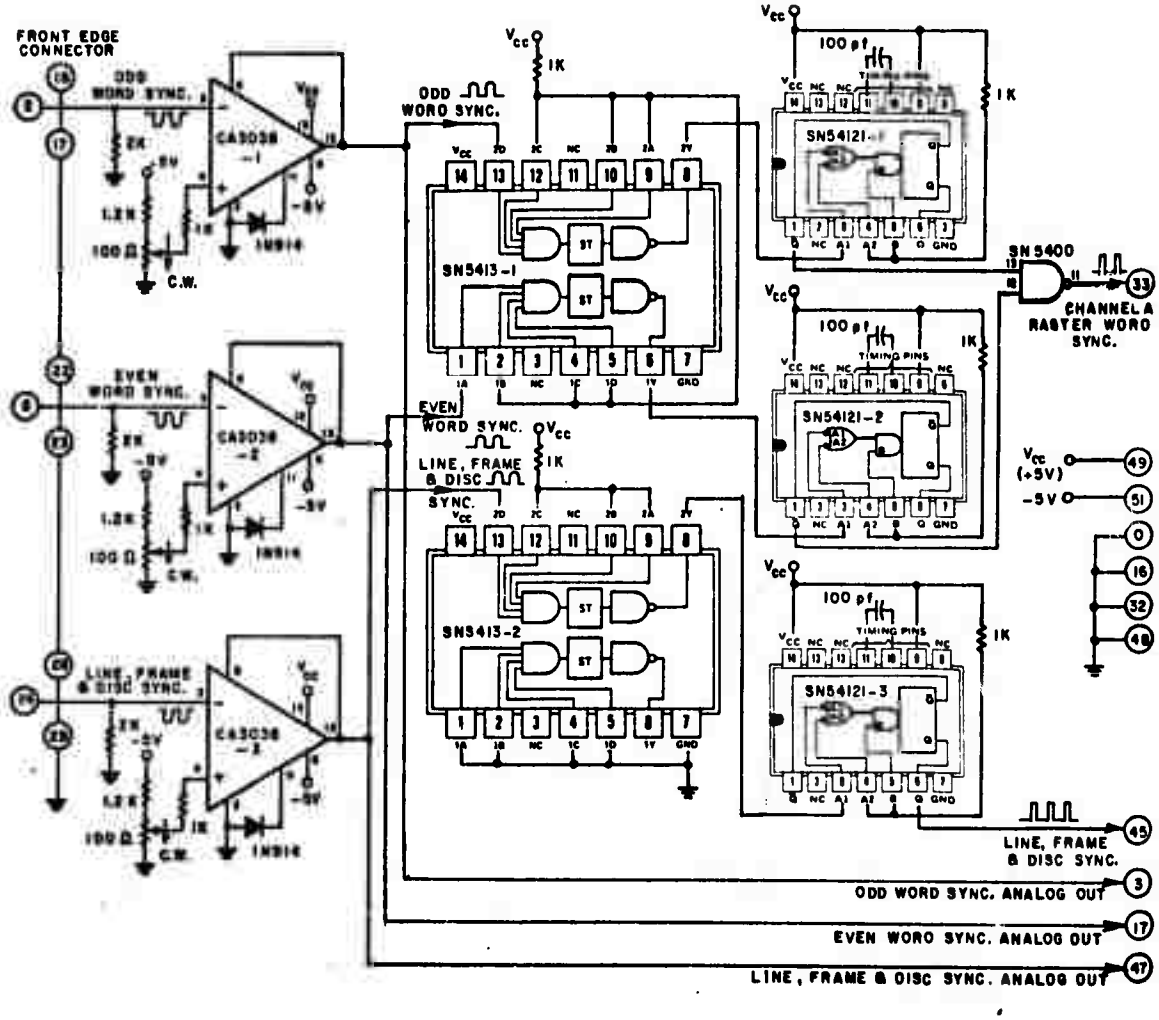


Fig. 33. Scanner sync generator logic diagram.

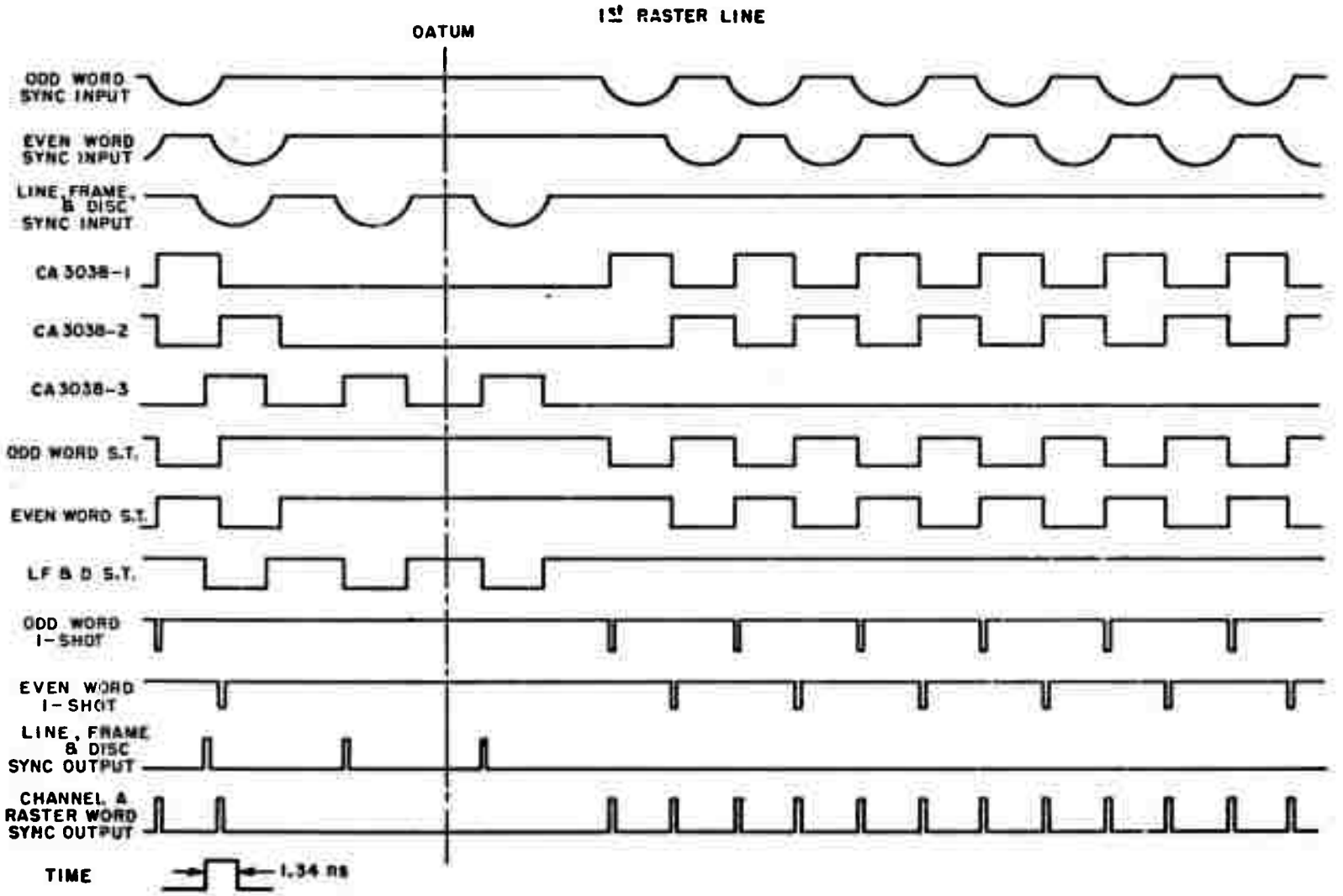
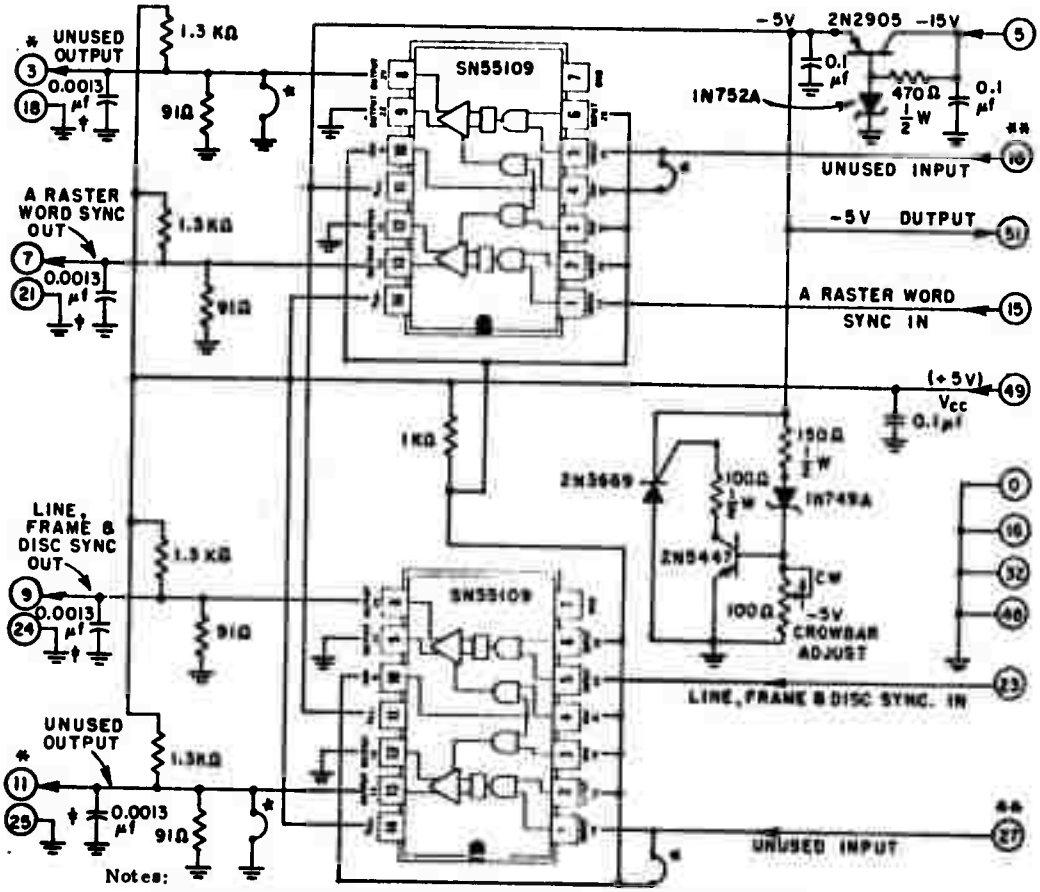


Fig. 34. Scanner sync generator timing diagram.



Notes:

*these jumpers are connected on unused spare inputs and outputs

**spare inputs

*spare outputs

†capacitor value = Total Distributed Capacity of output line. Value shown is for 100 ft. of RG62B/U.

Fig. 35. Line drivers schematic diagram.

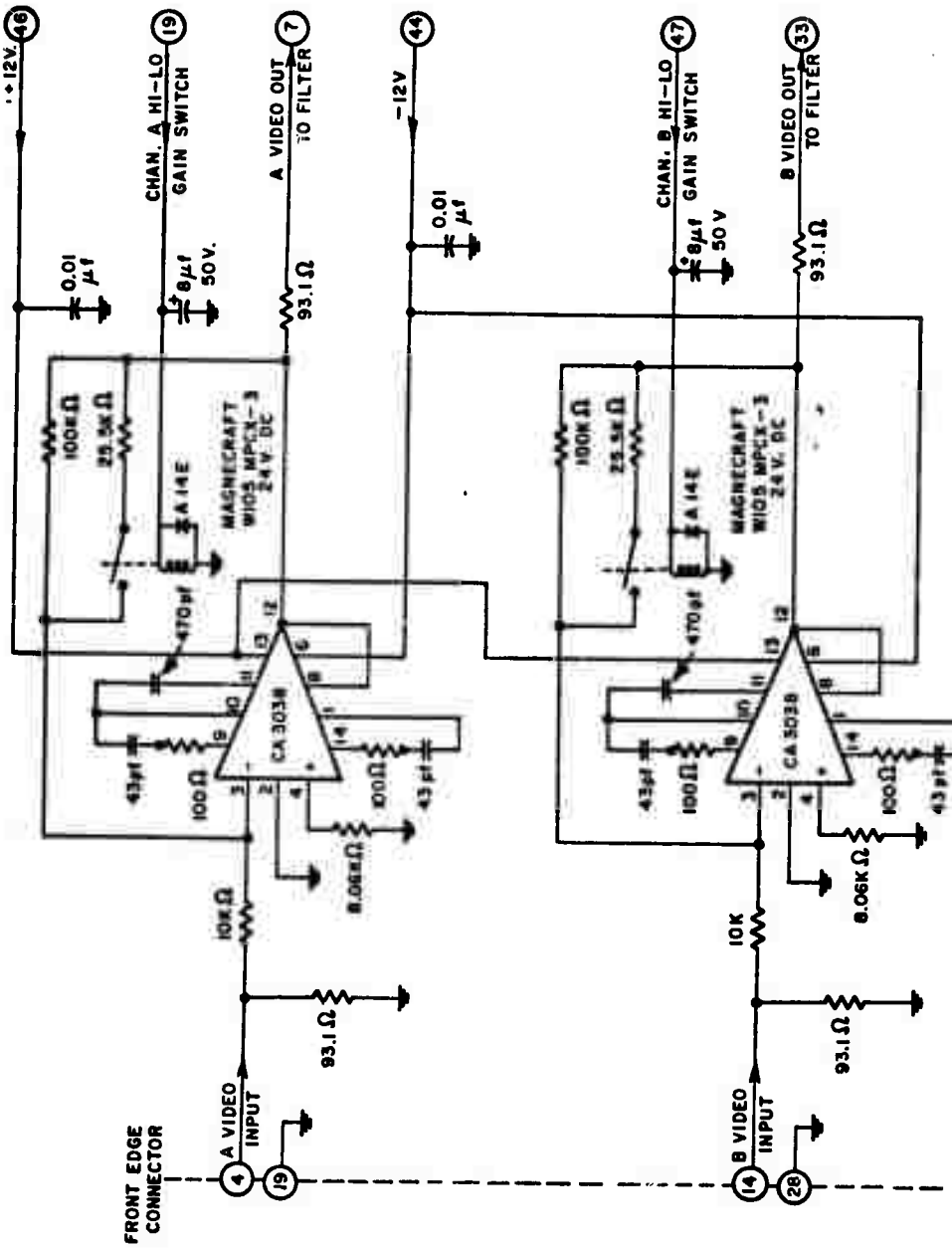


Fig. 36. Video filter amplifier schematic diagram.

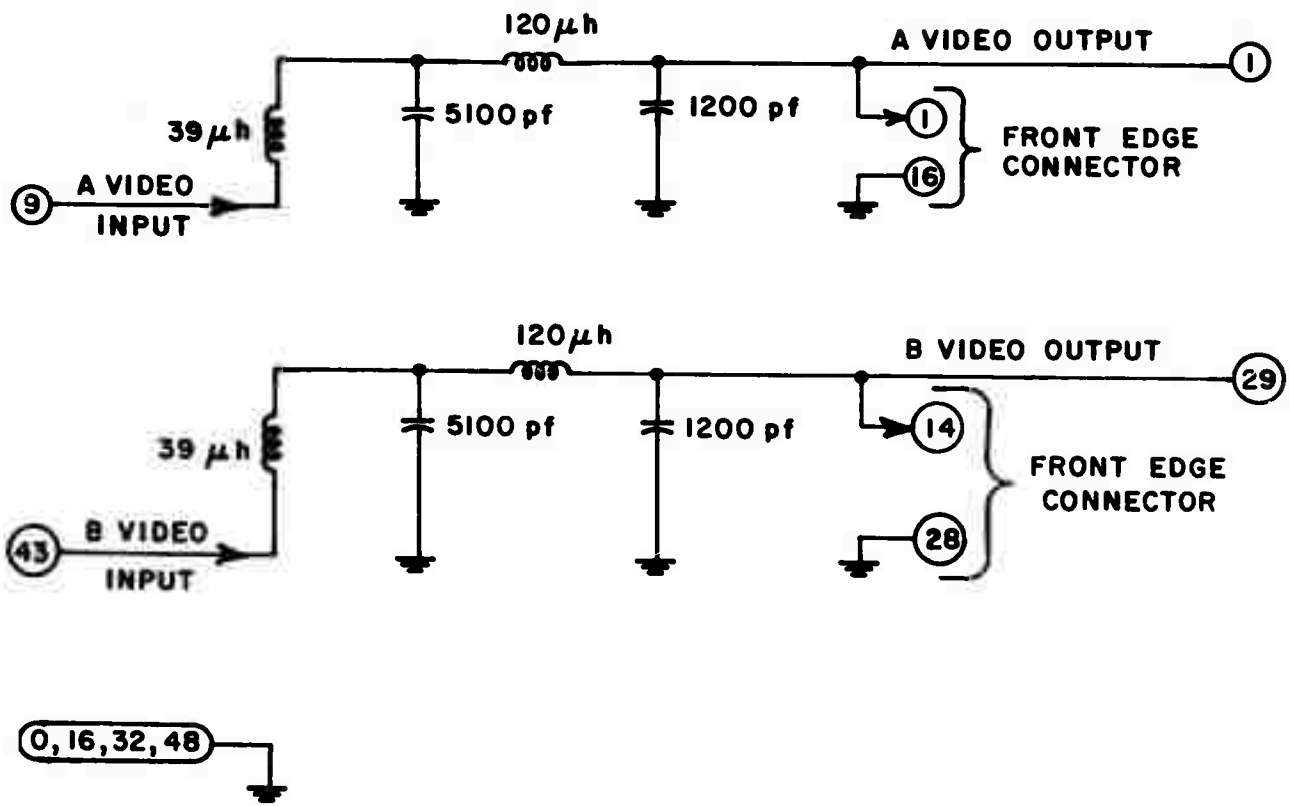


Fig. 37. Video filter schematic diagram.

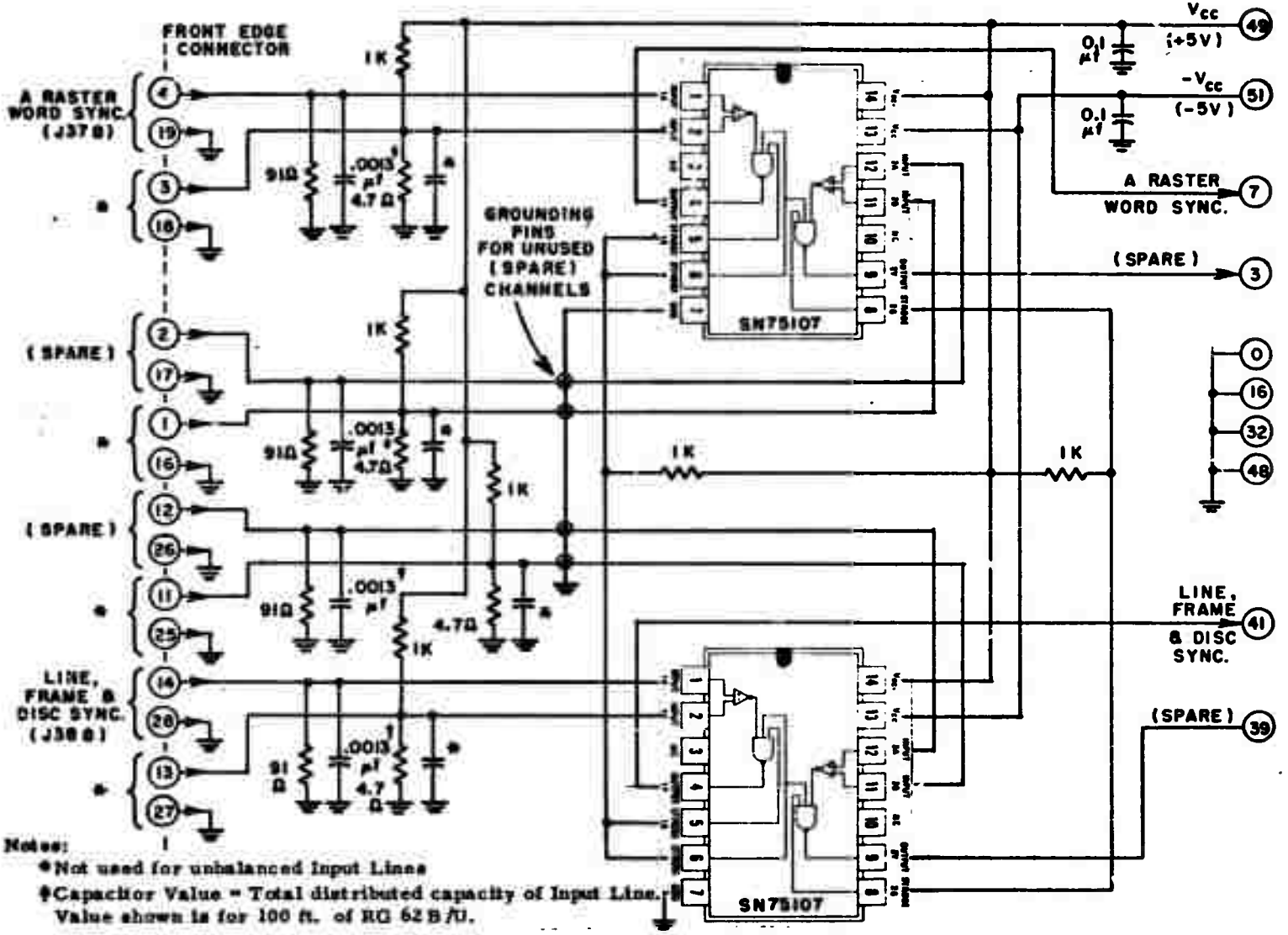


Fig. 38.. Line receivers schematic diagram.

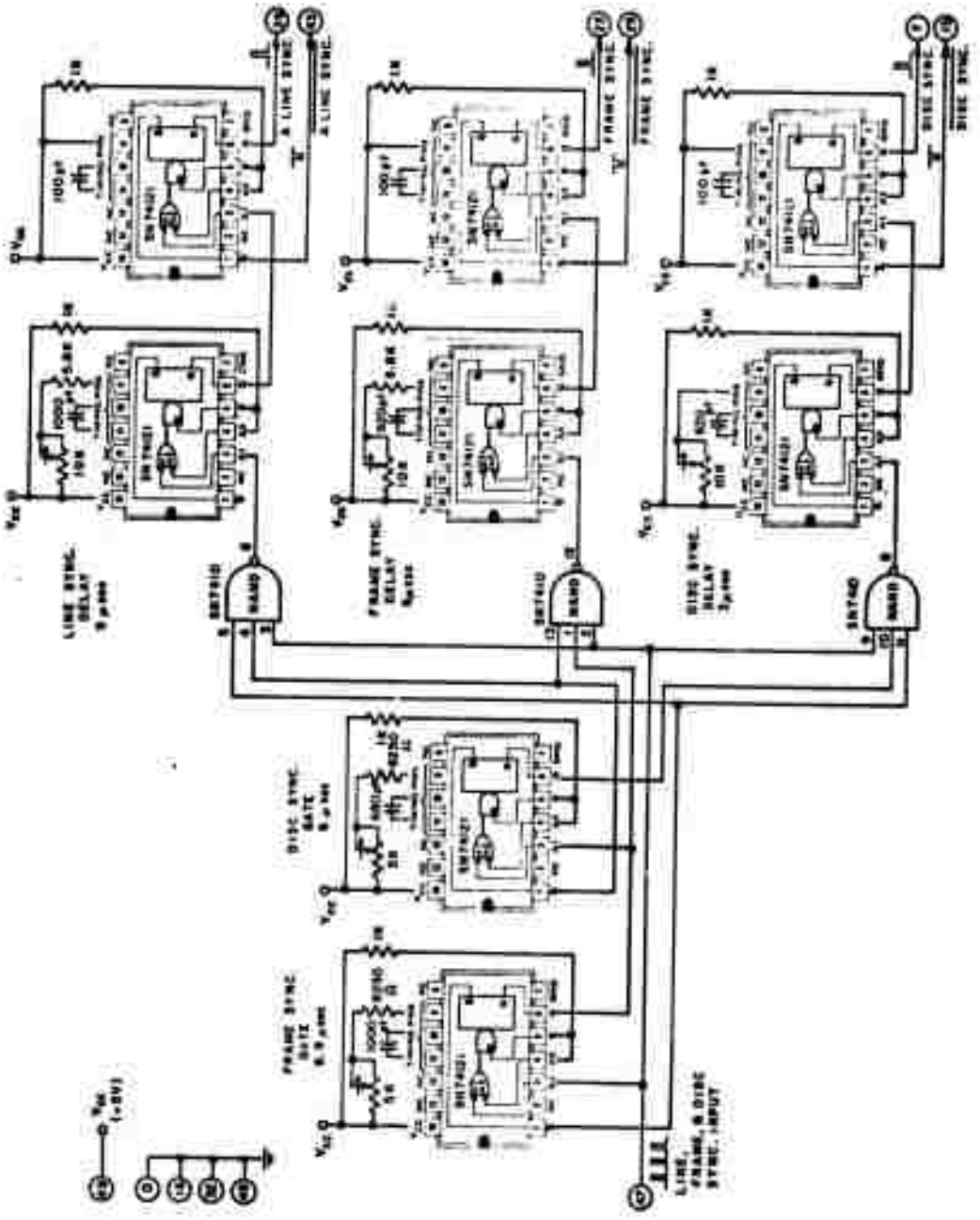


Fig. 39. Sync separator schematic diagram.

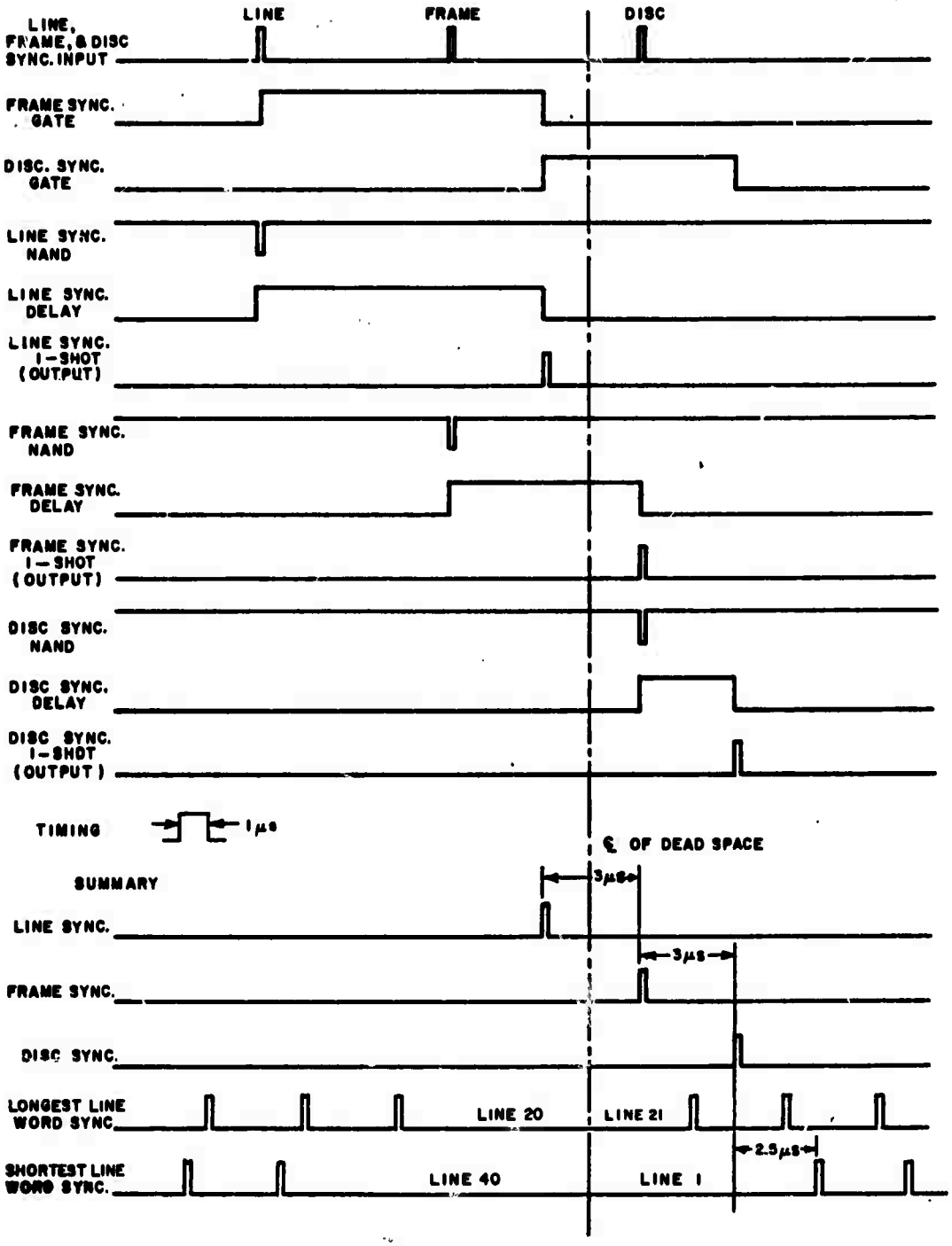


Fig. 40. Sync separator timing diagram.

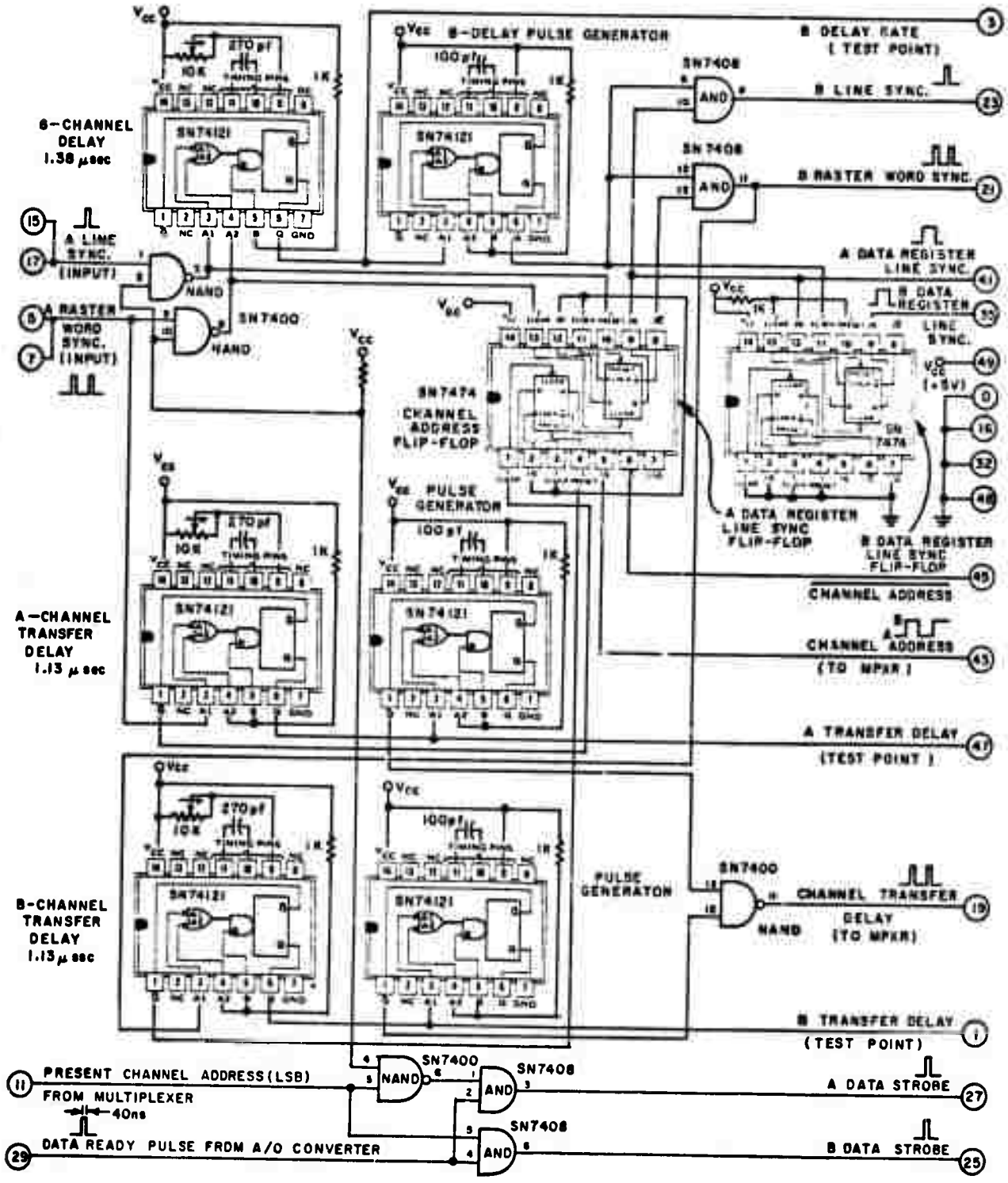


Fig. 41. B-sync generator and digital data demultiplexer schematic diagram.

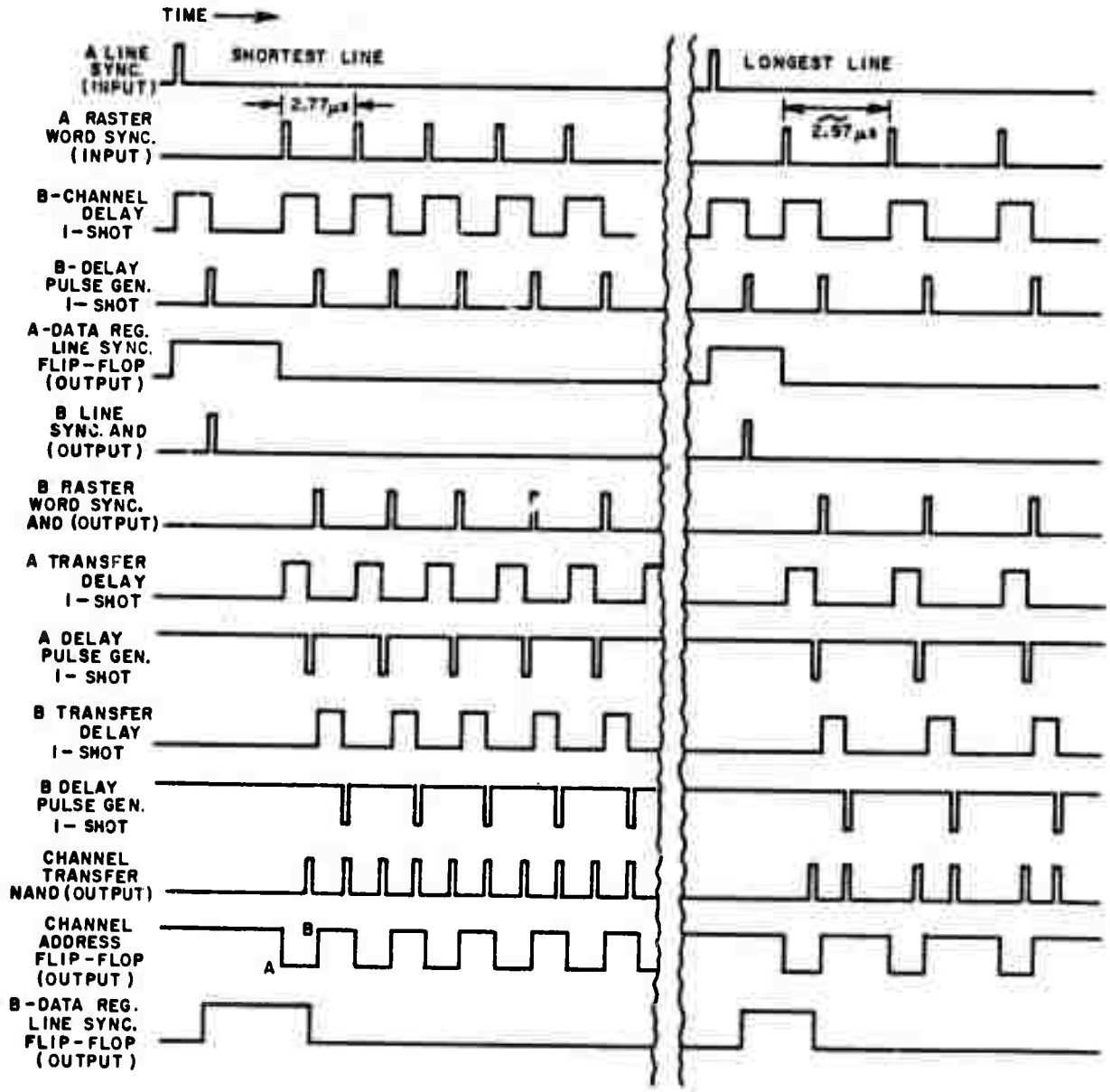


Fig. 42. B-sync generator timing diagram.

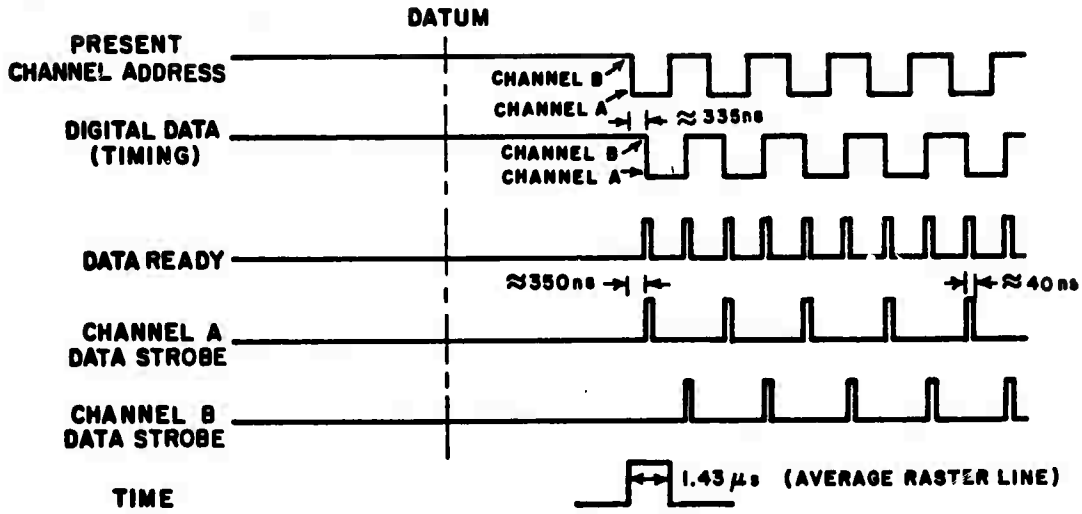


Fig. 43. Digital data demultiplexer timing diagram.

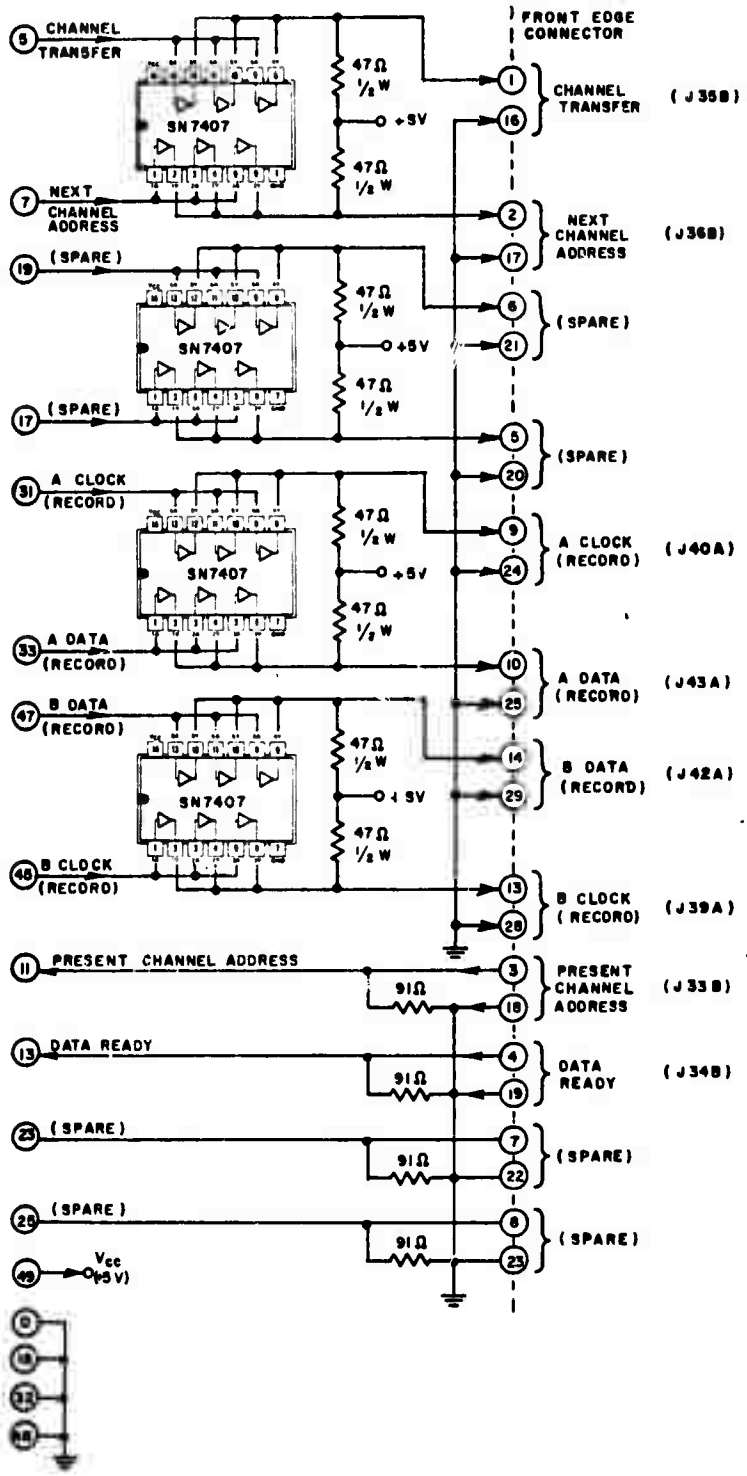


Fig. 44. Co-ax driver schematic diagram.

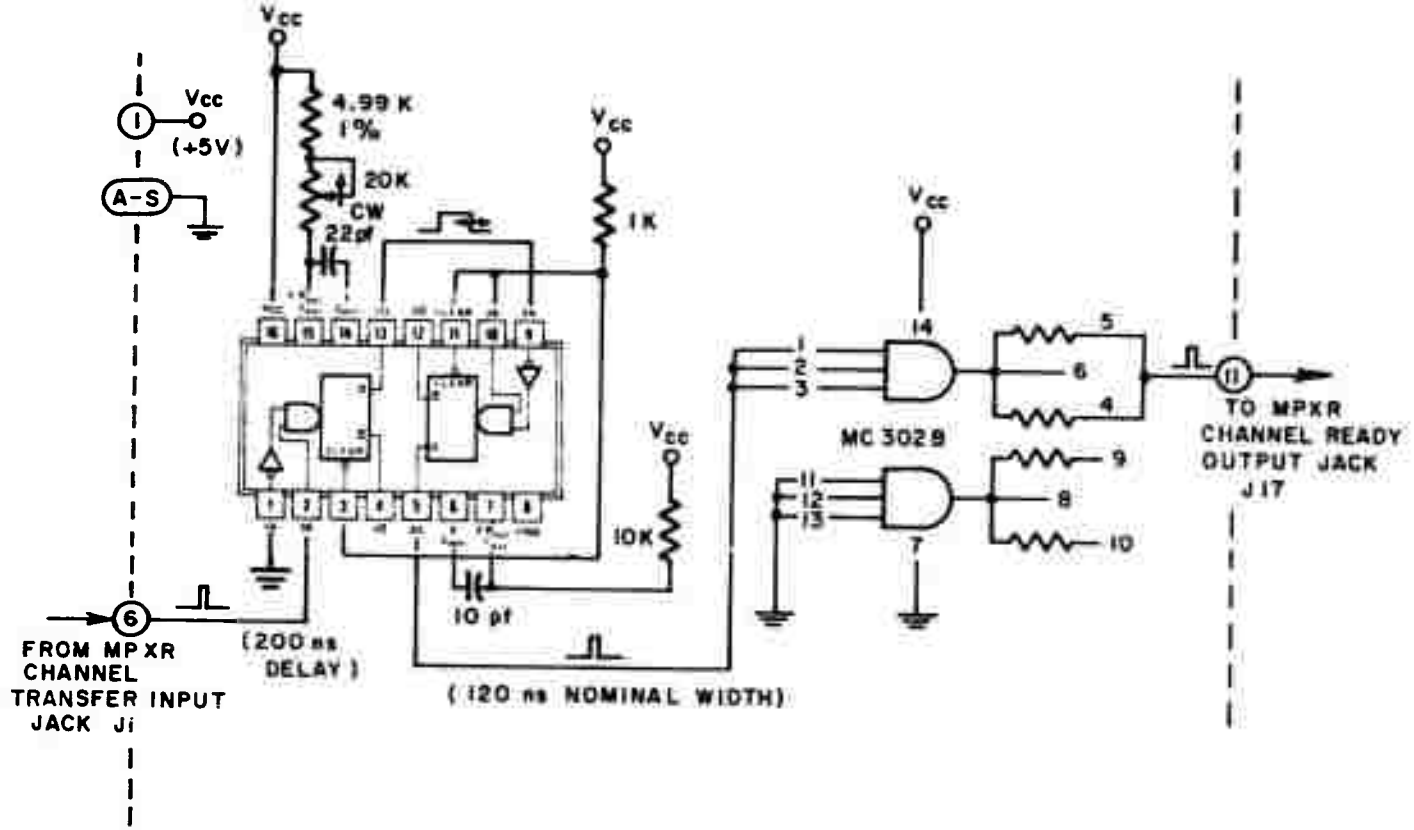


Fig. 45. Channel ready delay and driver for MUX 810 multiplexer.

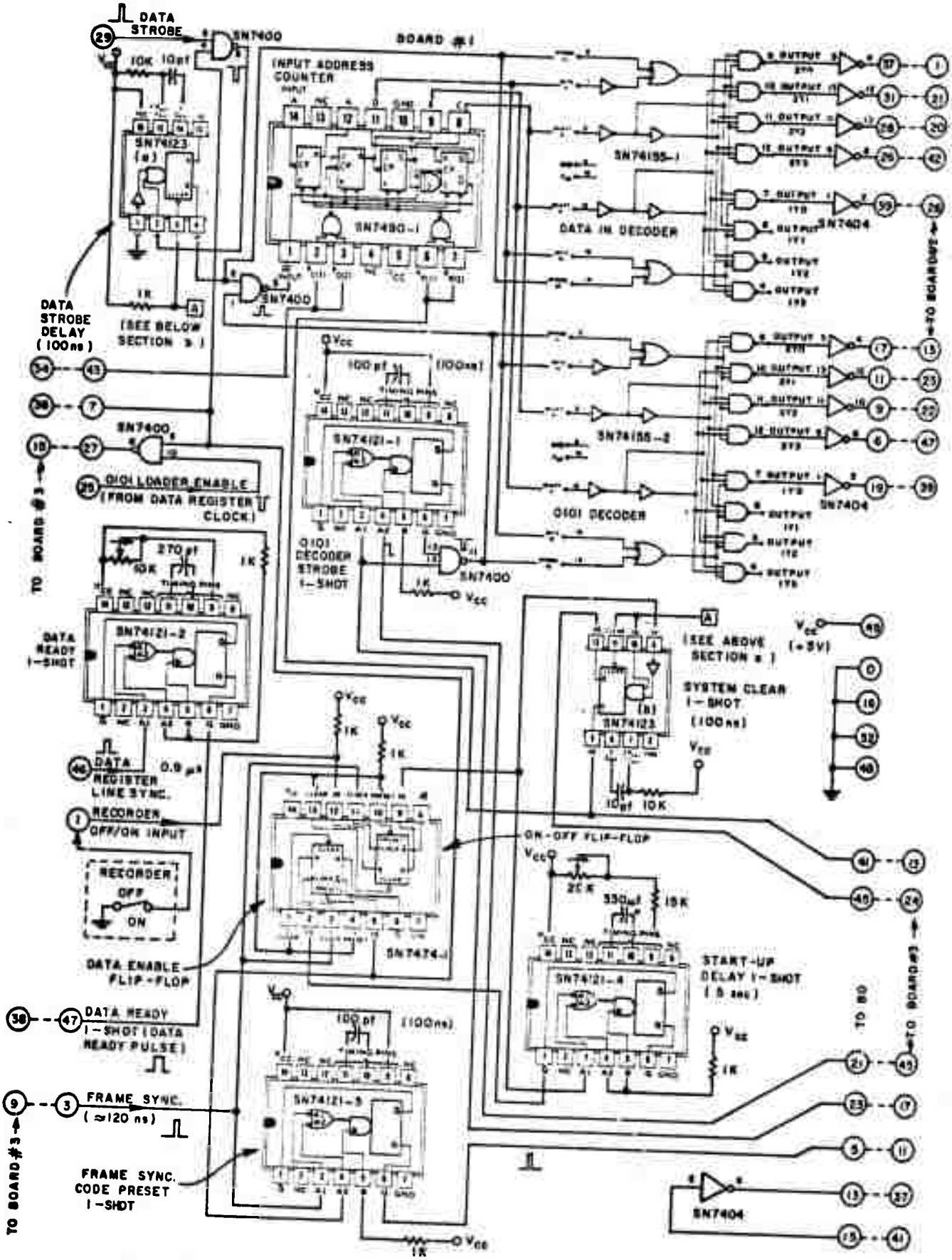


Fig. 46. Parallel input-serial output encoder logic diagram. Sheet 1 - Circuit board #1.

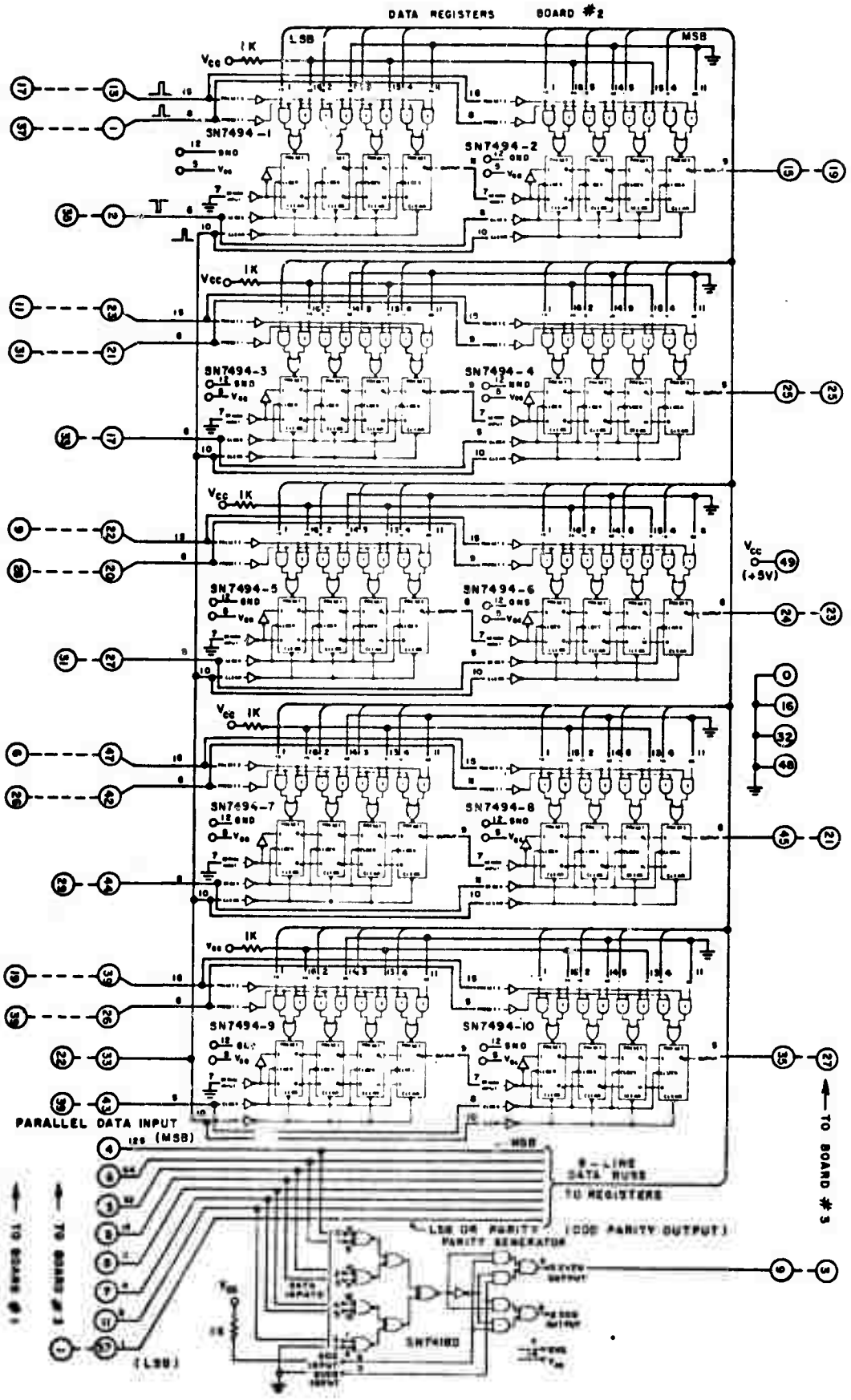


Fig. 46. Parallel input-serial output encoder logic diagram. (cont.)
Sheet 2 - Circuit board #2.

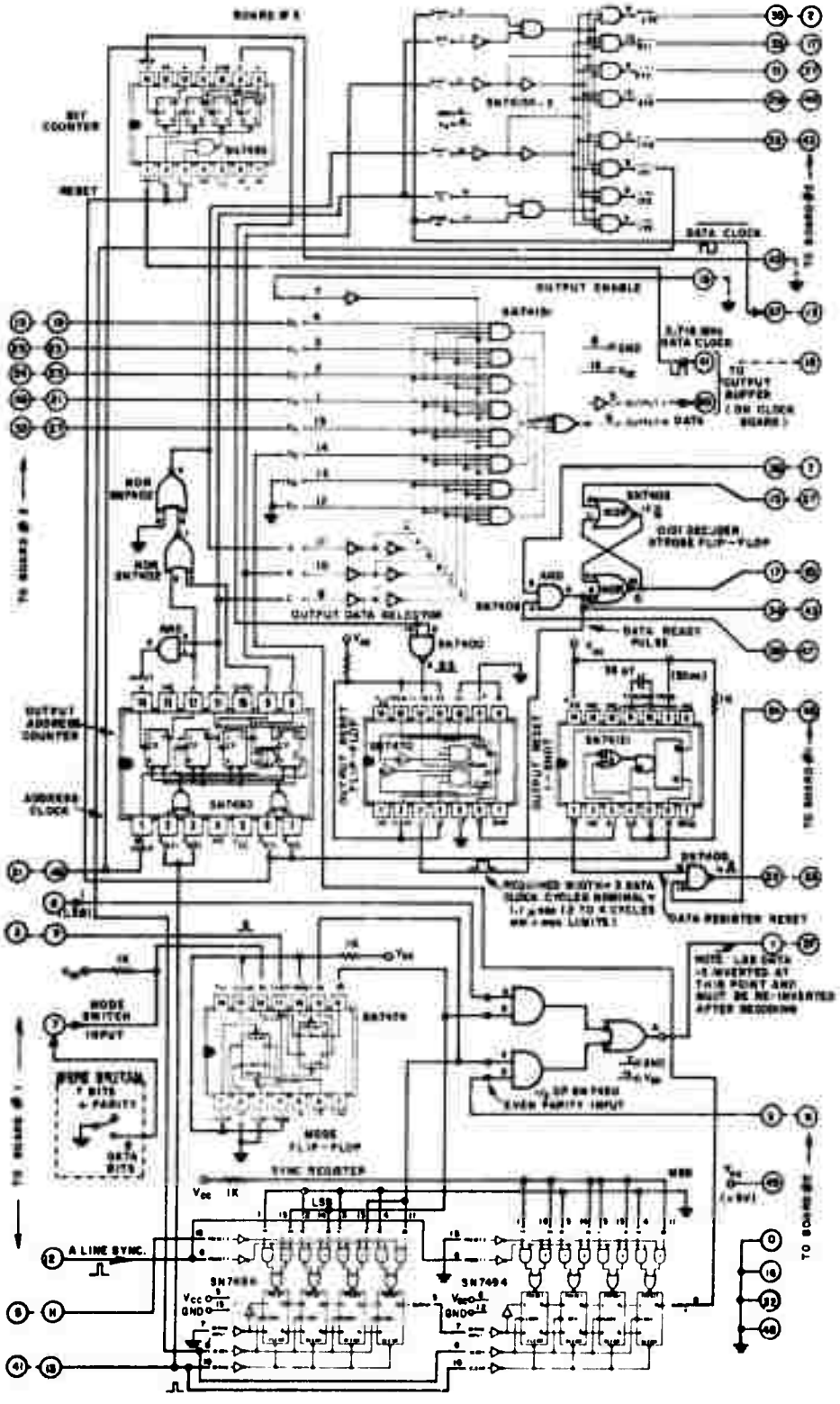


Fig. 46. Parallel input-serial output encoder logic diagram. (cont.)
Sheet 3 - Circuit board #3.

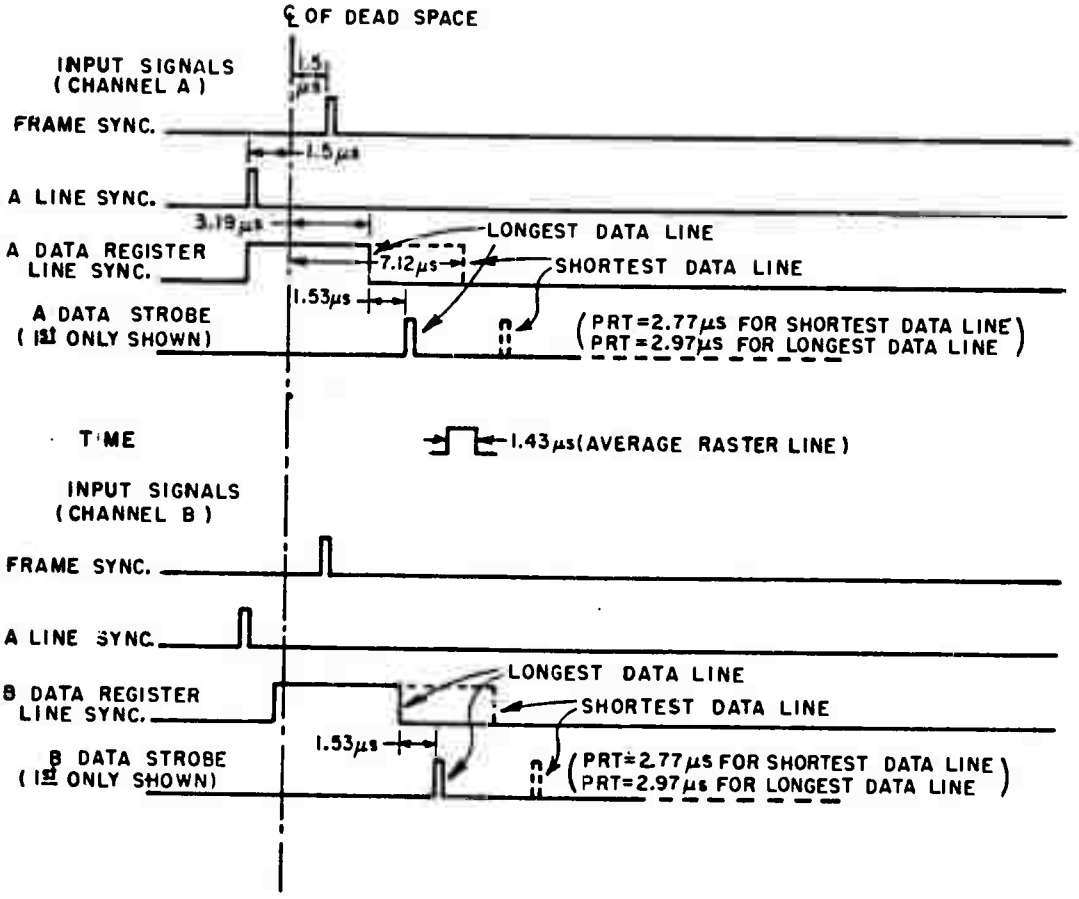


Fig. 47. Parallel input-serial output encoder timing diagram.
Sheet 1 - Input signals.

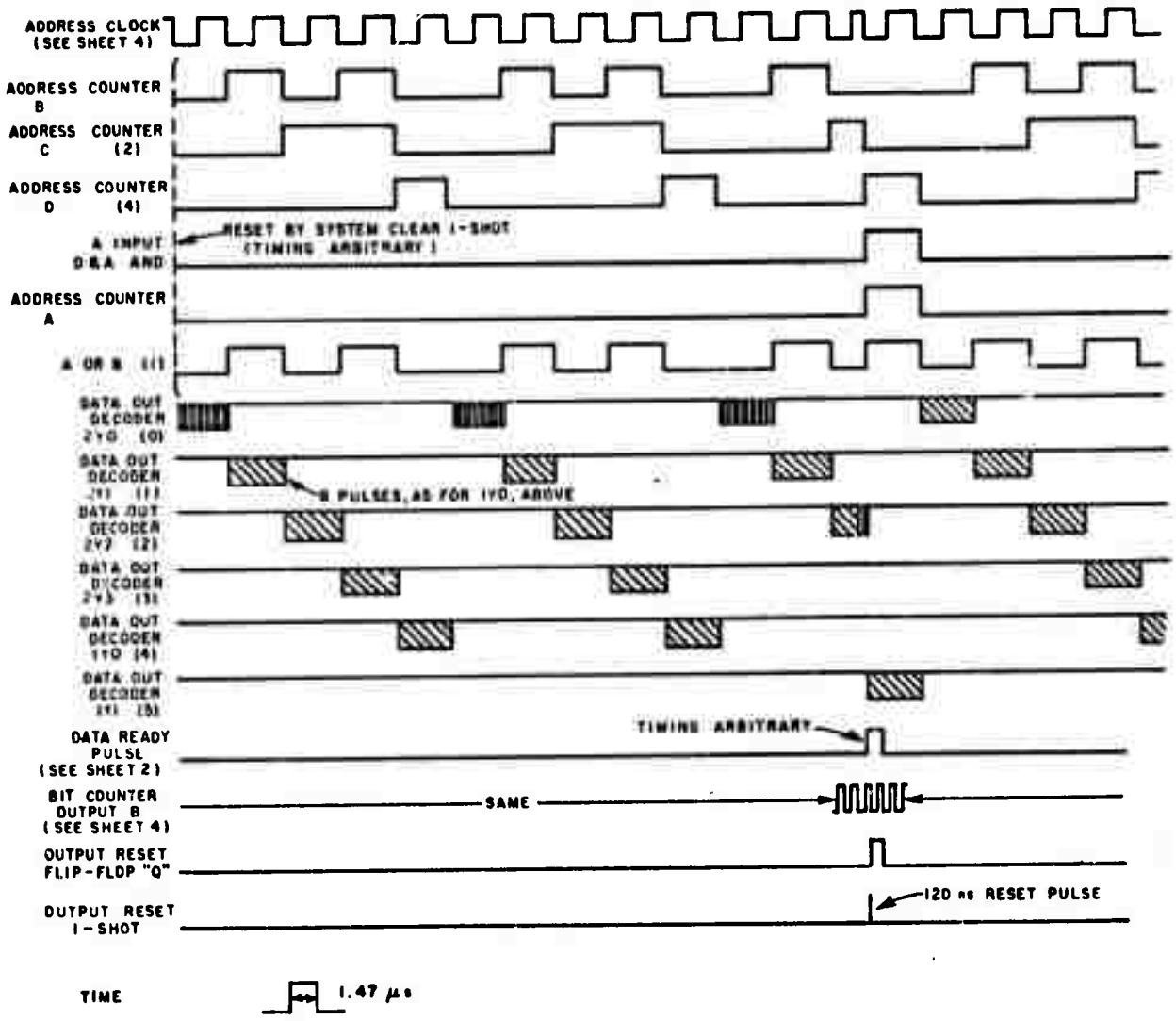


Fig. 47. Parallel input-serial output encoder timing diagram. (cont.)
Sheet 2 - Data input.

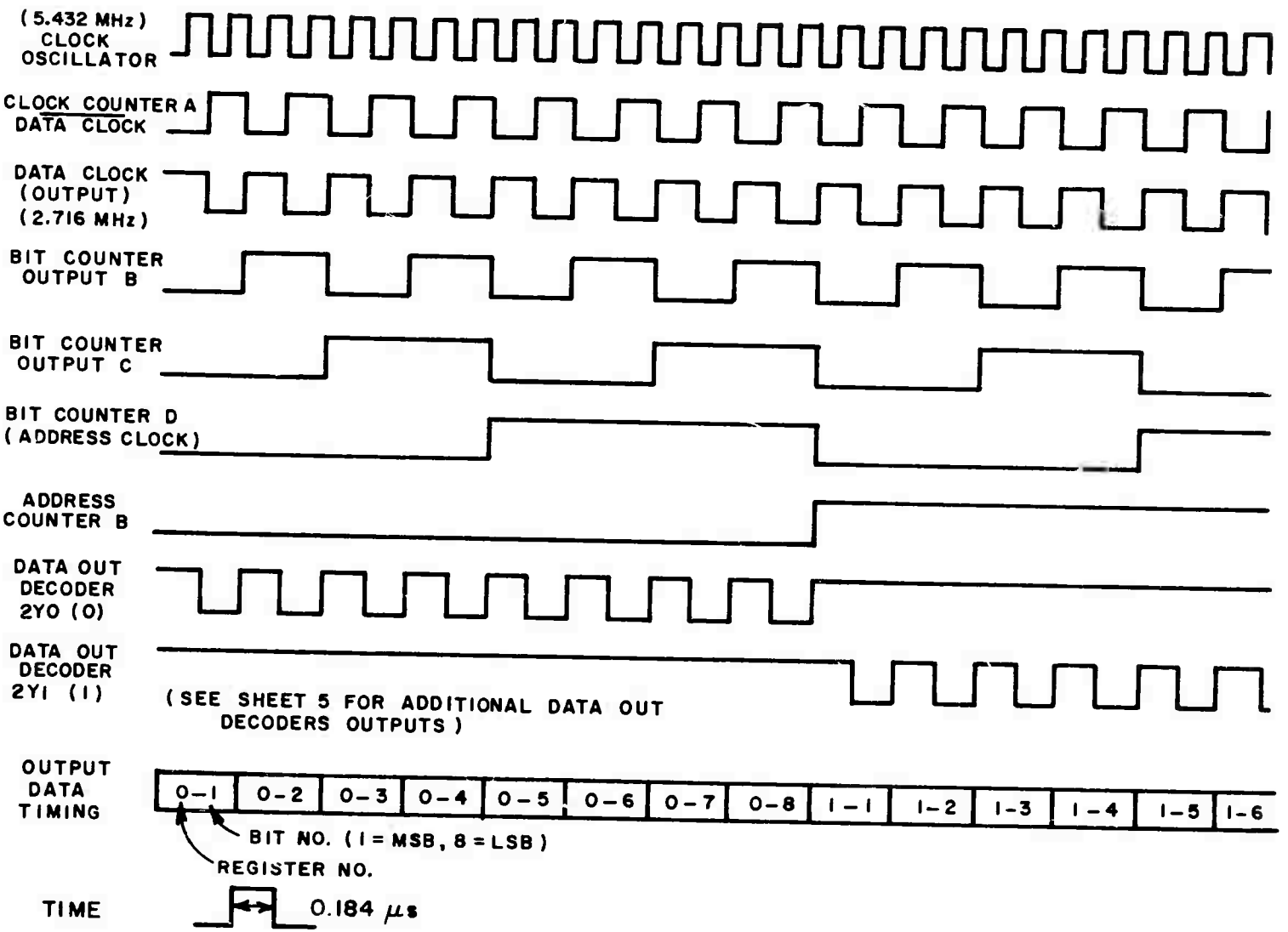


Fig. 47. Parallel input-serial output encoder timing diagram. (cont.)
Sheet 3 - Turn- on, turn-off, and mode switching.

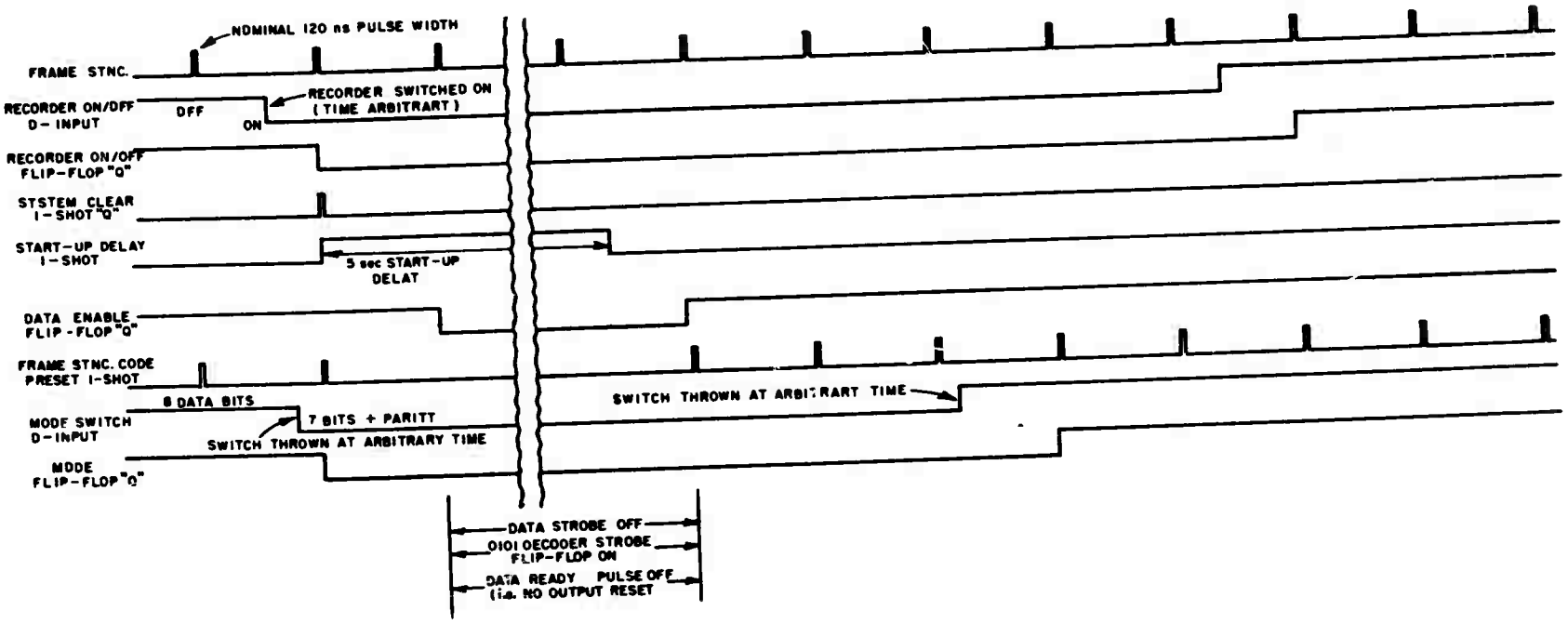


Fig. 47. Parallel input-serial output encoder timing diagram. (cont.)
Sheet 4 - Clock and output counters.

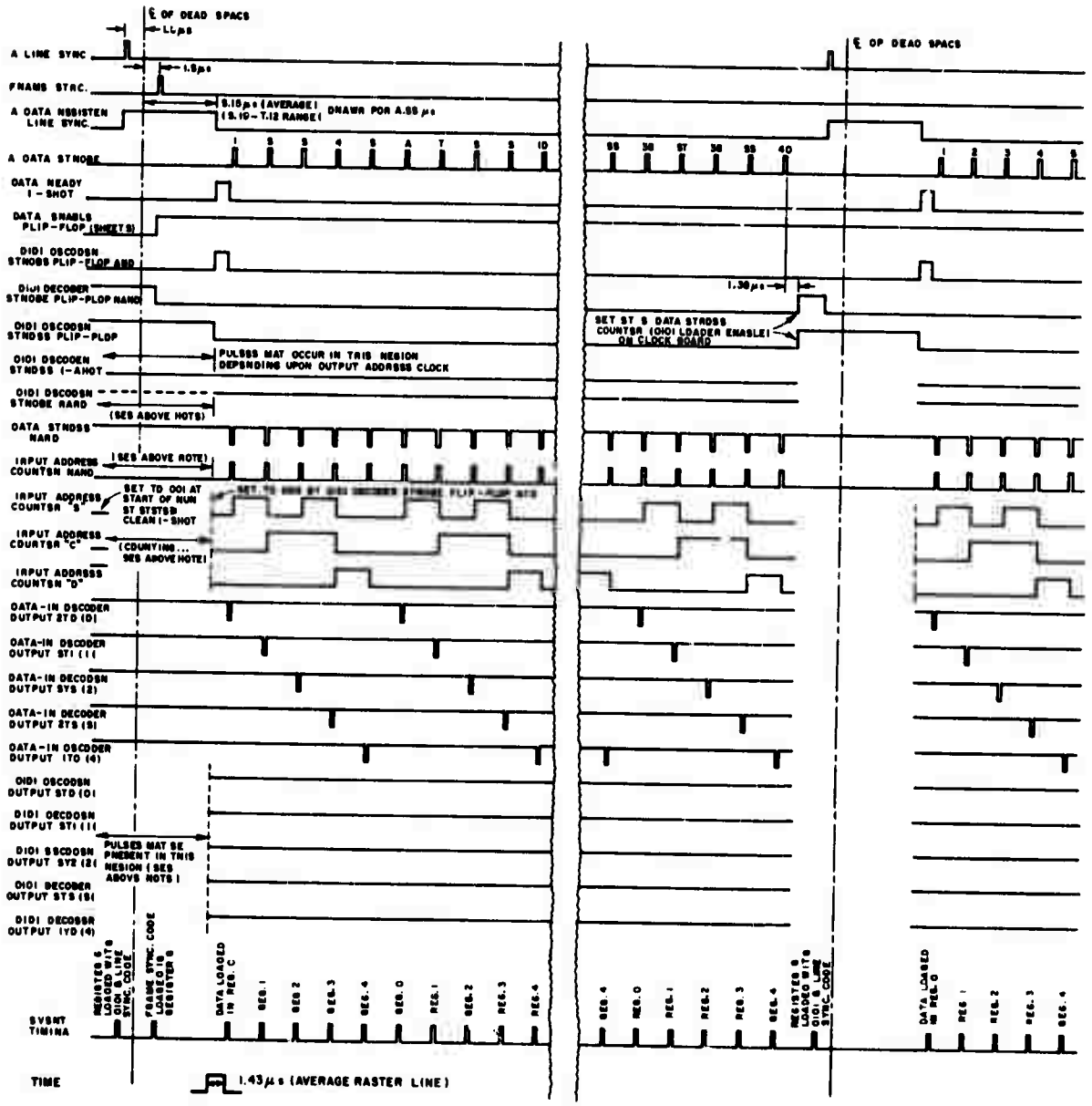


Fig. 47. Parallel input-serial output encoder timing diagram. (cont.)
Sheet 5 - Data output.

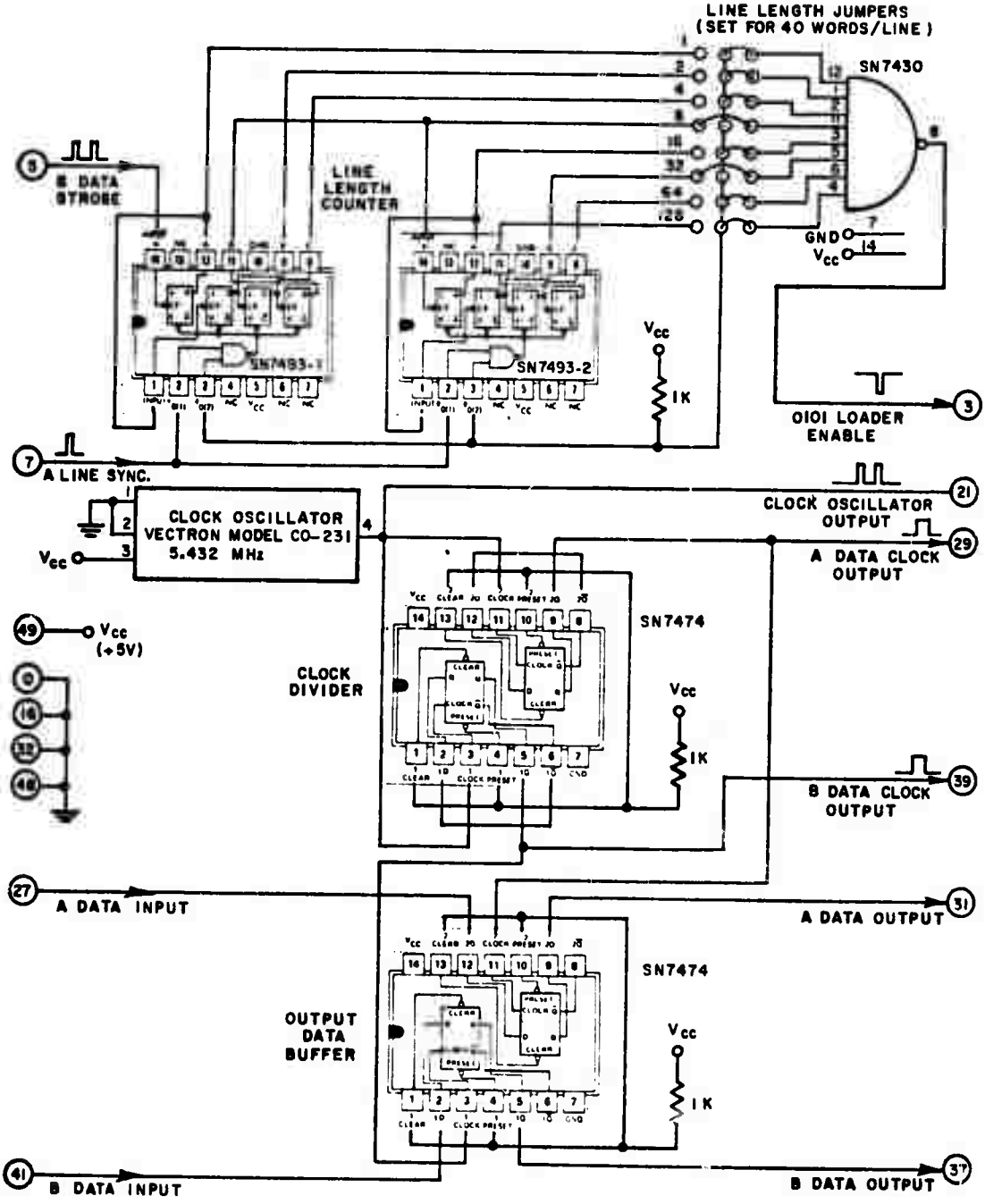


Fig. 48. Data register clock and output buffer logic diagram.

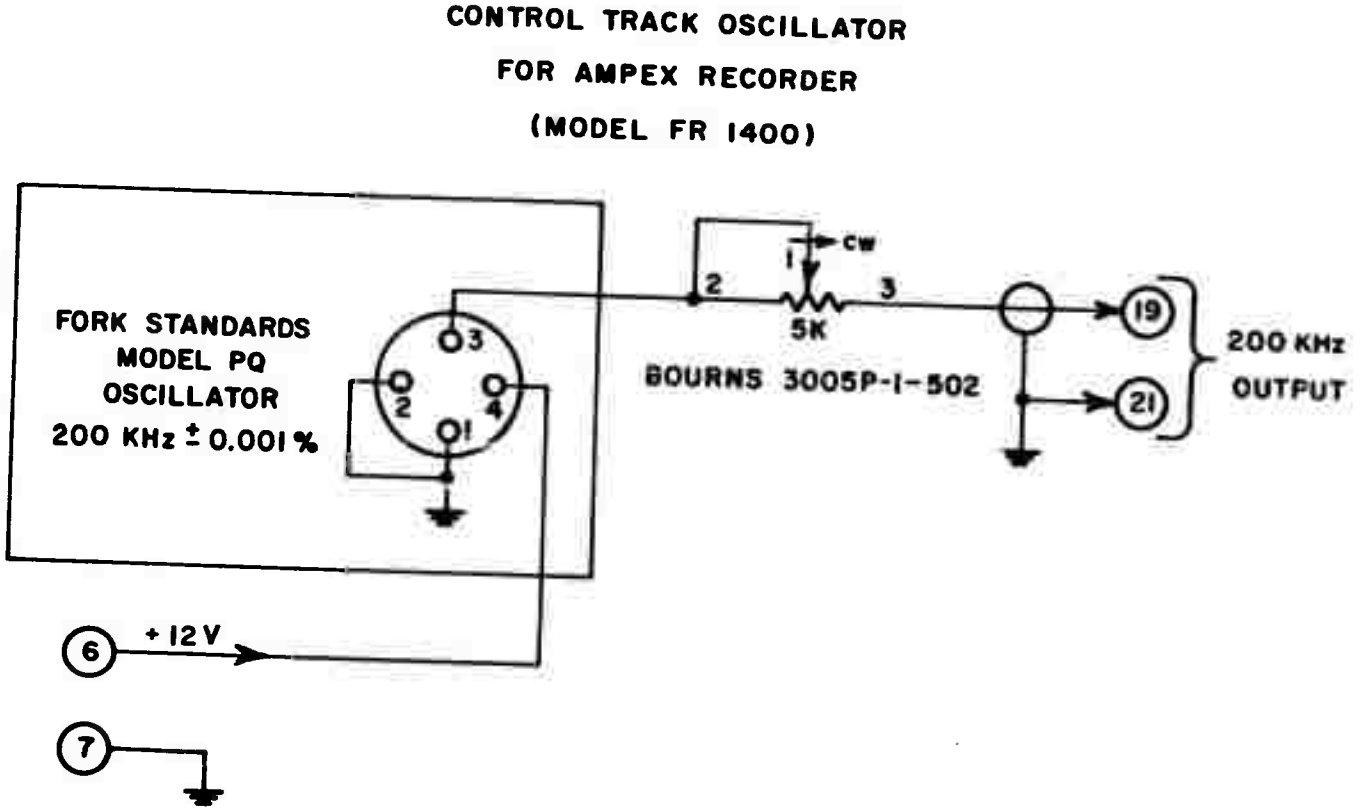


Fig. 49. Control track oscillator schematic diagram.

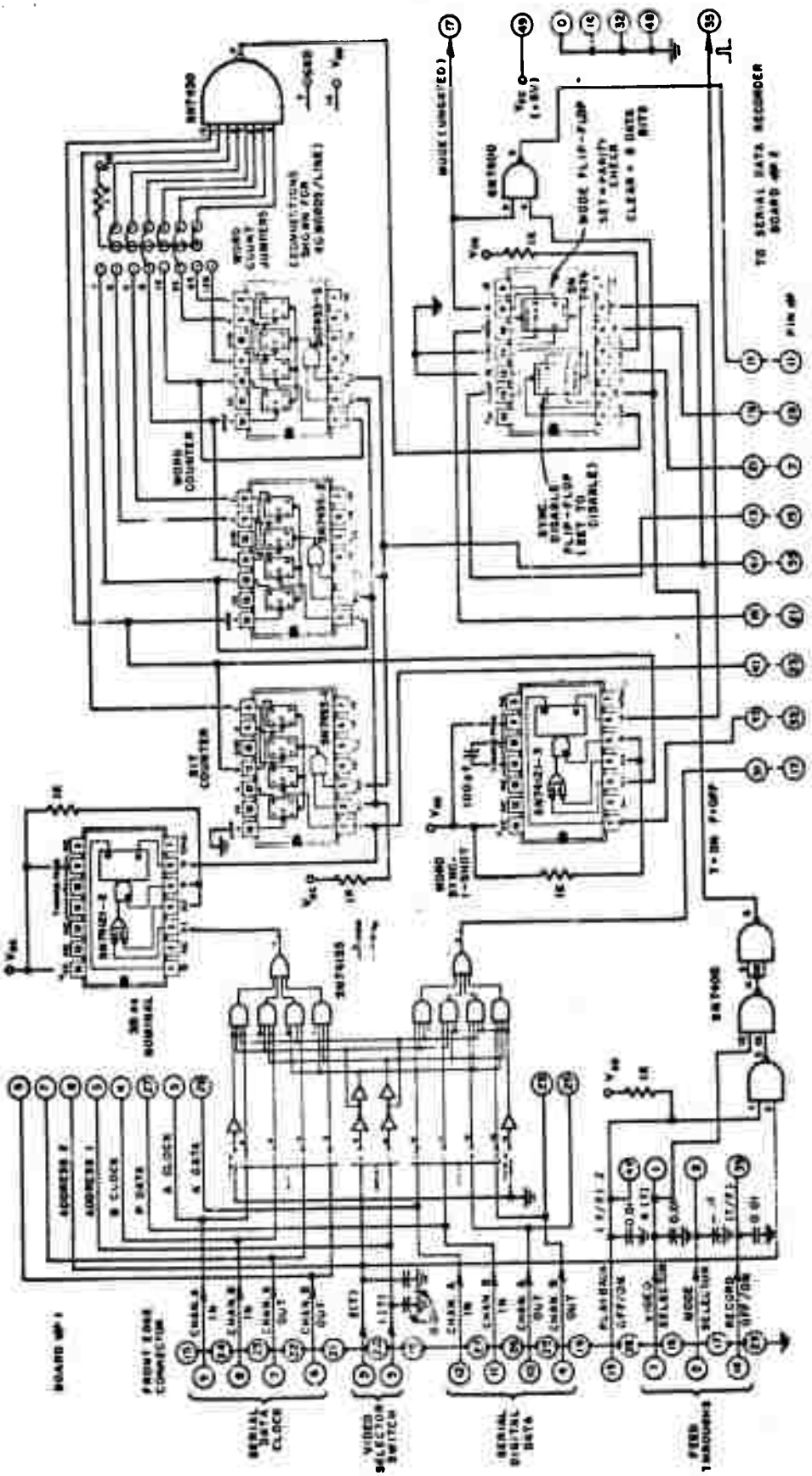


Fig. 50. Serial data decoder logic diagram.
Sheet 1 - Circuit board #1.

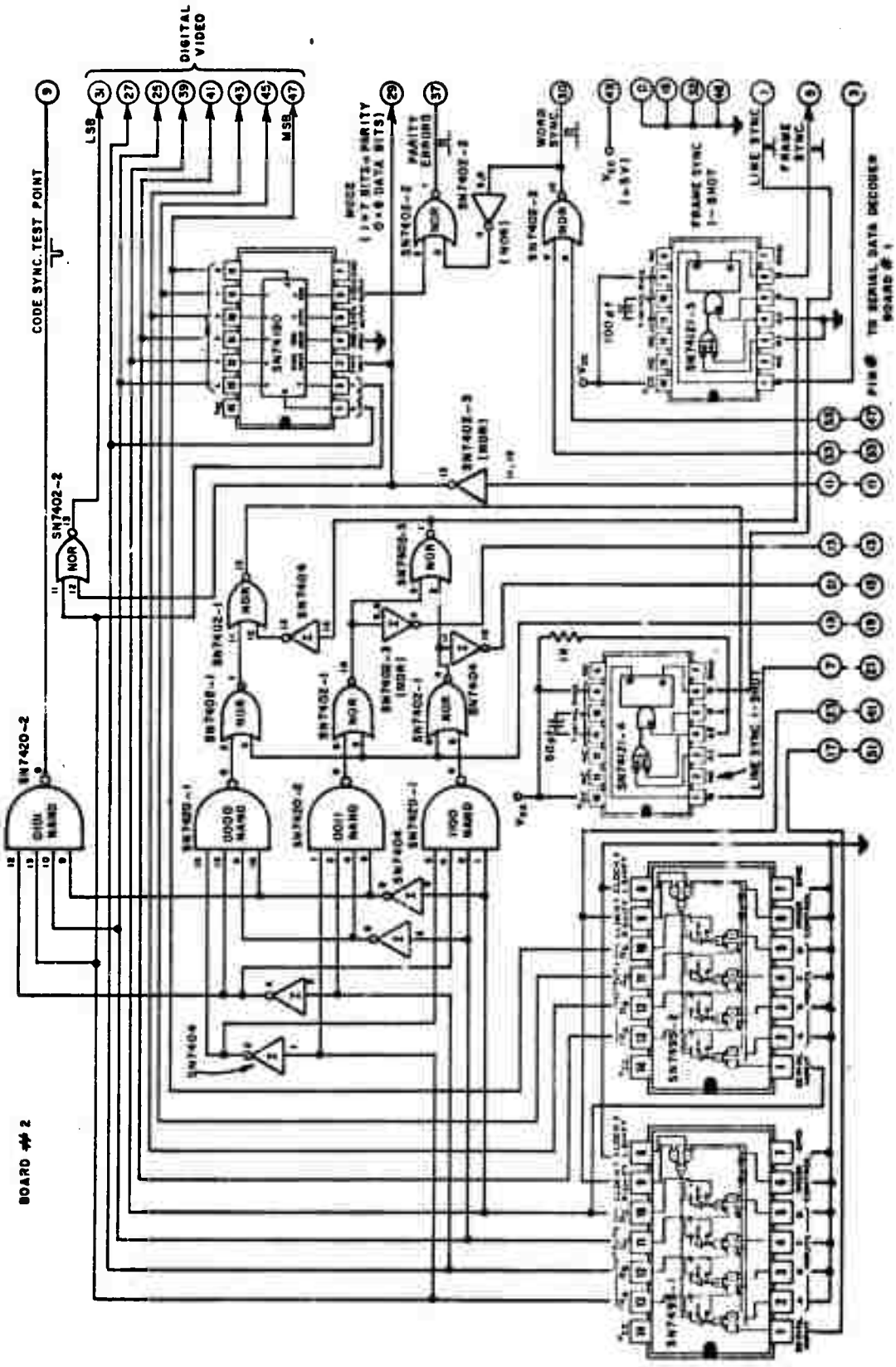


Fig. 50. Serial data decoder logic diagram. (cont.)
Sheet 2 - Circuit board #2.

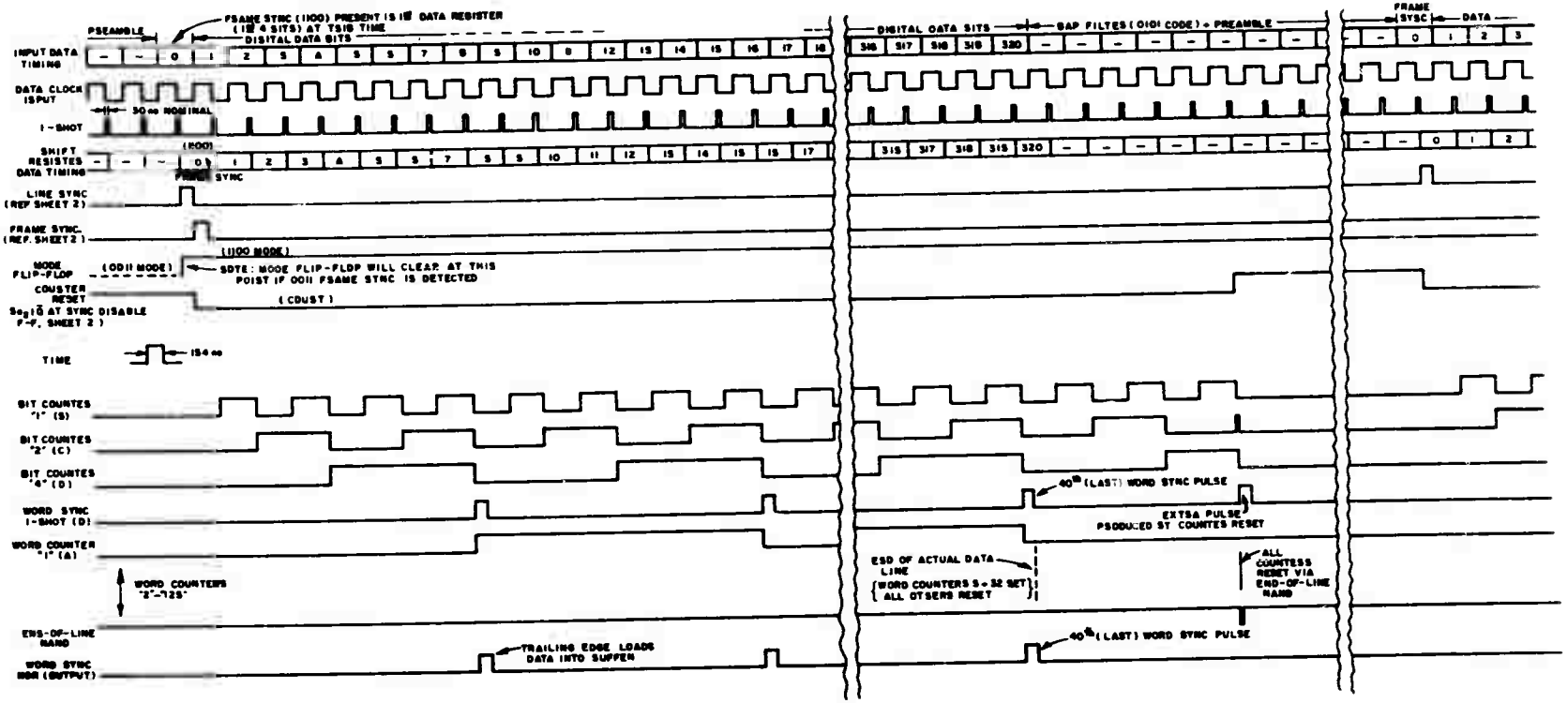


Fig. 51. Serial data decoder timing diagram.
Sheet 1 - Data timing.

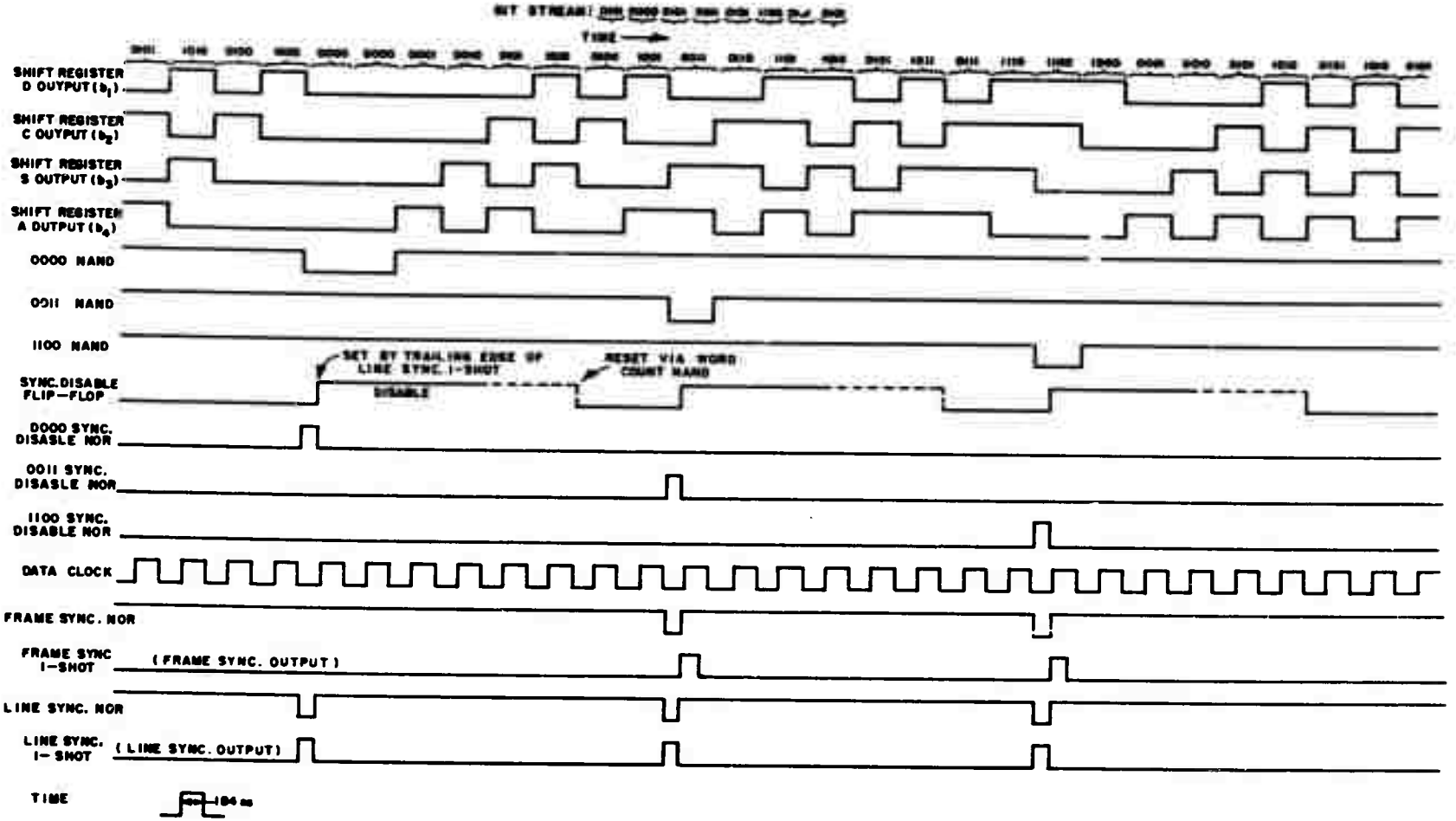


Fig. 51. Serial data decoder timing diagram. (cont.)
Sheet 2 - Sync decoder waveforms.

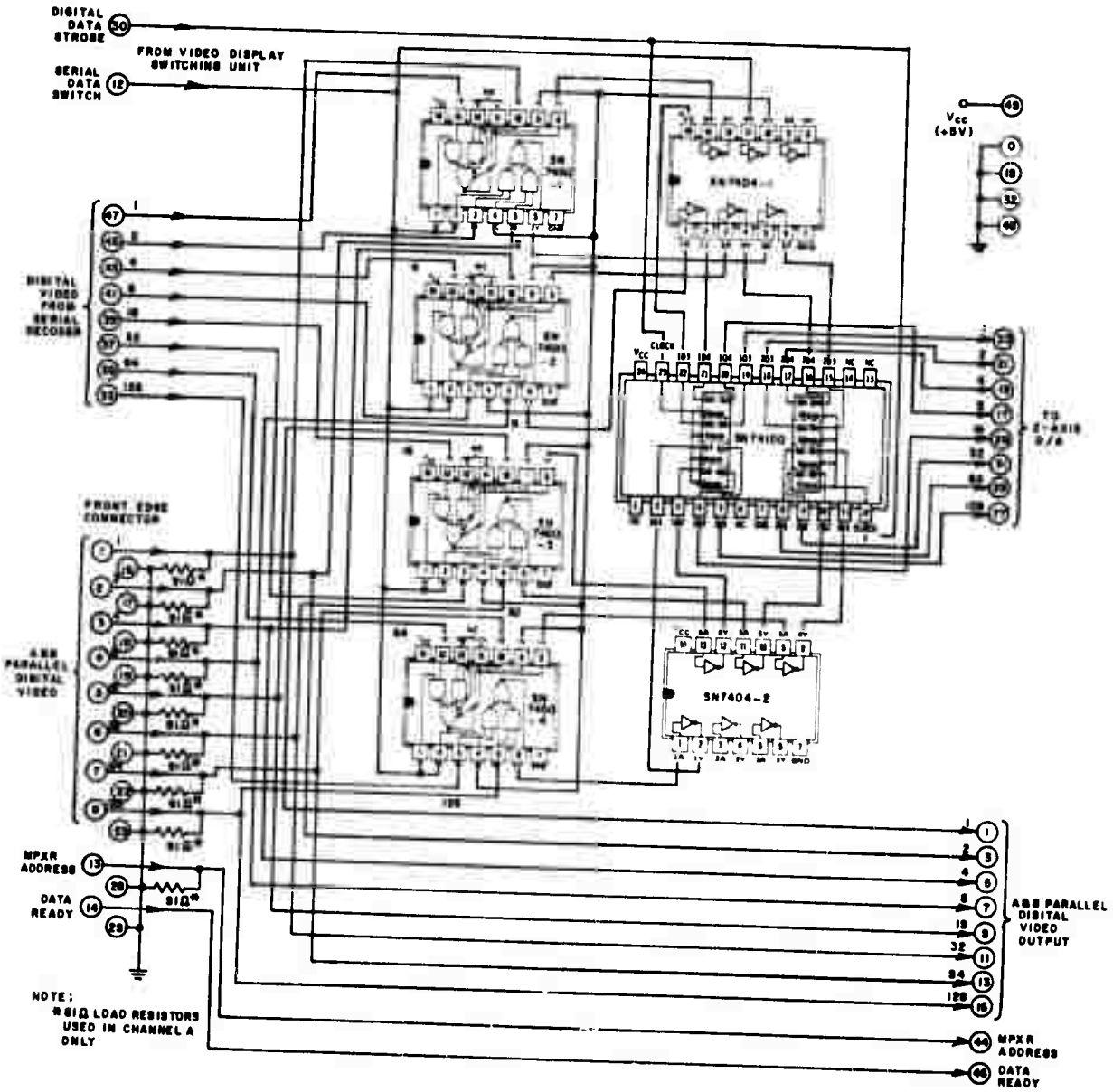


Fig. 52. Video data buffer logic diagram.

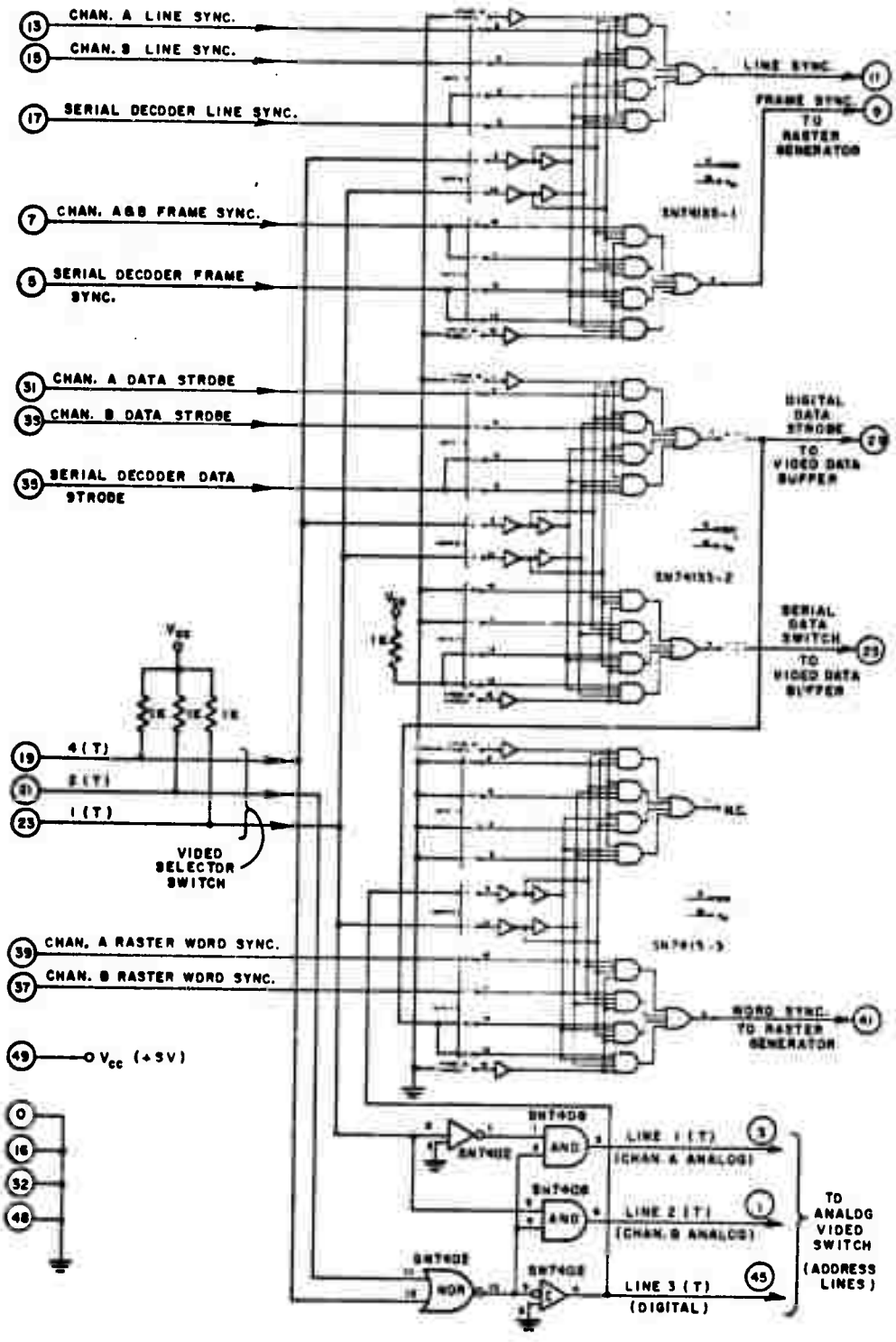
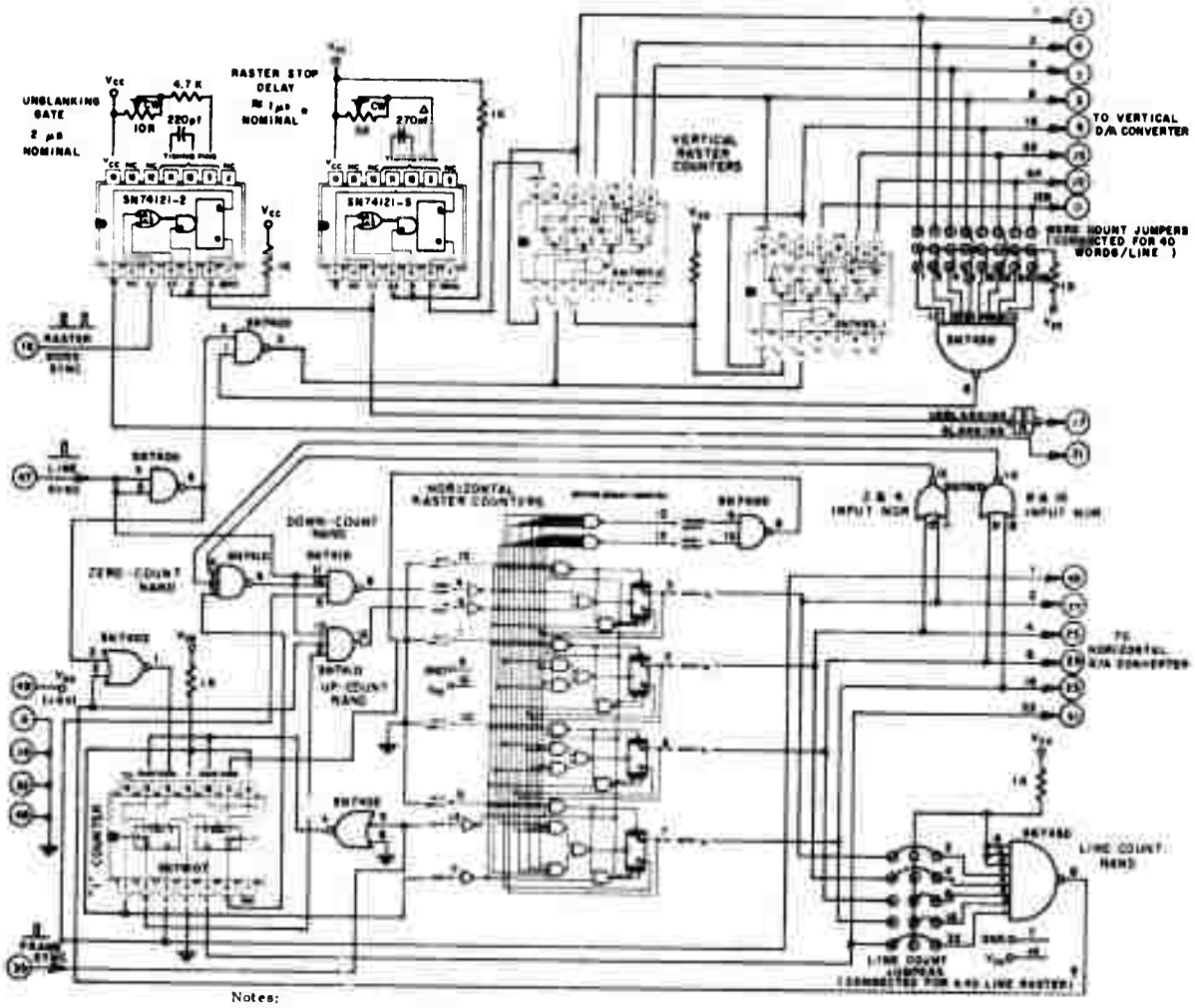


Fig. 53. Video display switching unit logic diagram.



Notes:

*Adjust Raster Step Delay to produce Raster step during blanking Pulse at Display Unit.

Δ 360 pf in Scanner Control Unit CU-2.

†Line-Count Jumper Connections Input Sum [S = N - 2] where N = No. of Raster Lines.

Fig. 54. Raster generator logic diagram.

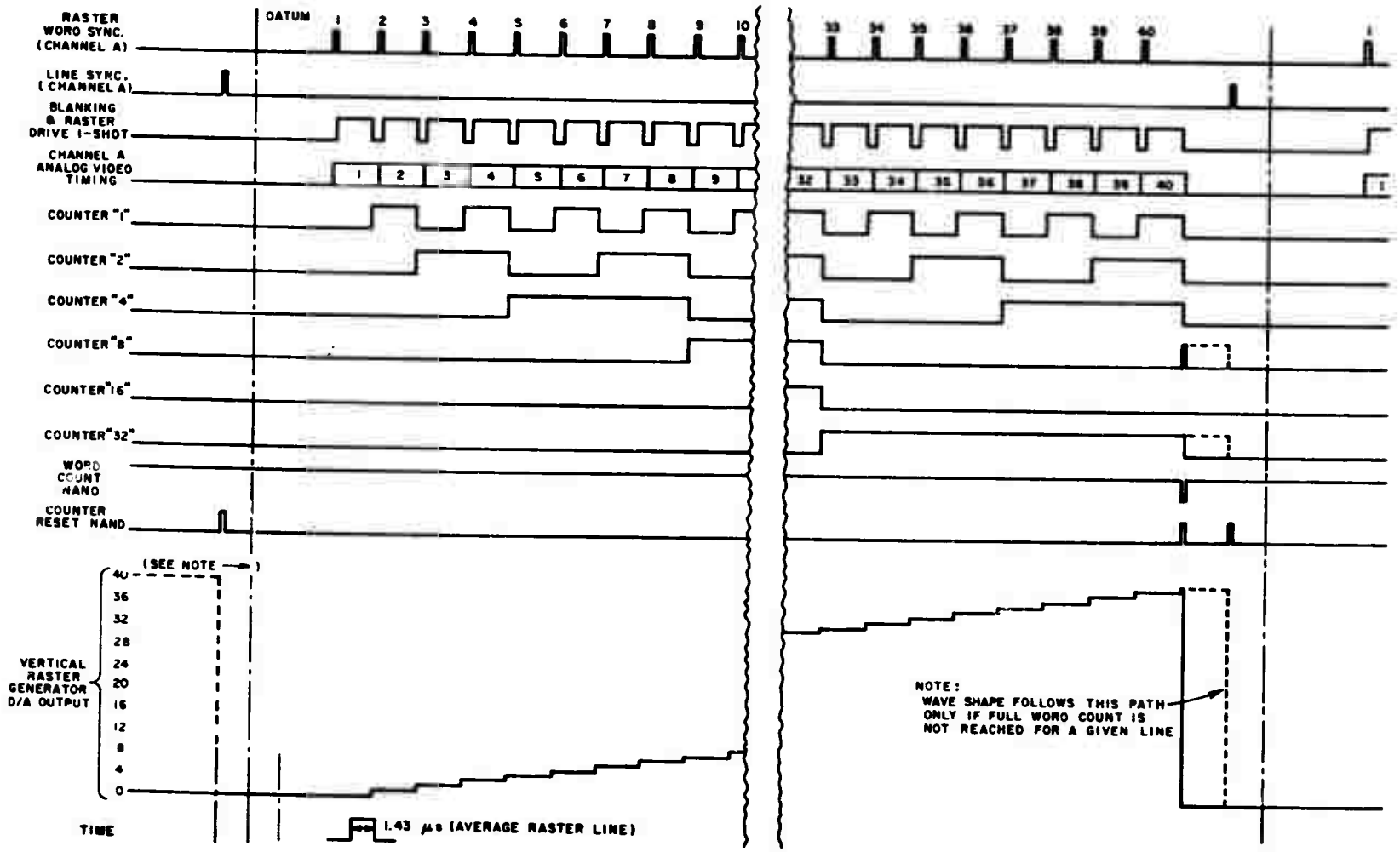


Fig. 55. Raster generator timing diagram.
Sheet 1 - Vertical raster generator.

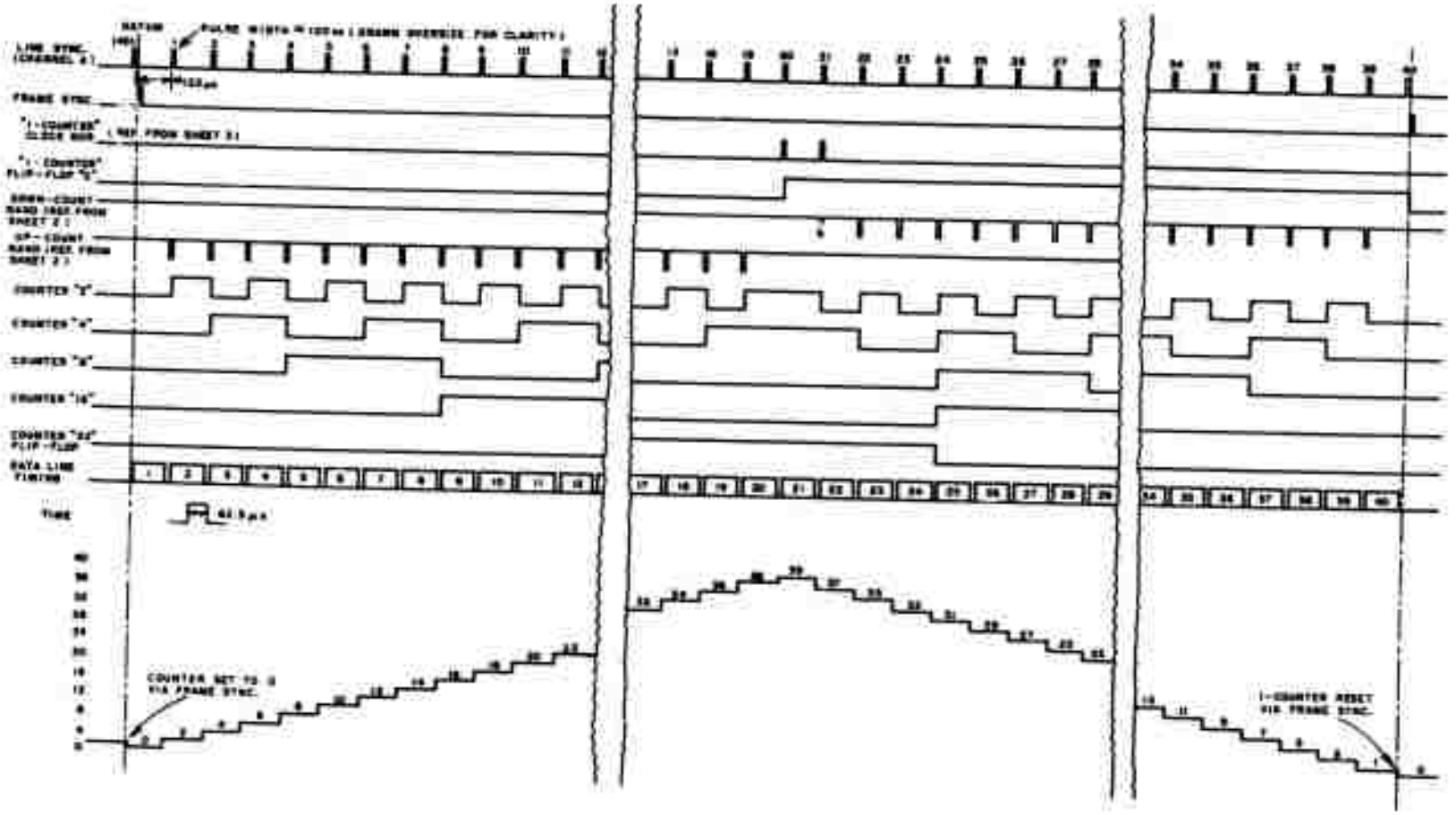


Fig. 55. Raster generator timing diagram. (cont.)
Sheet 2 - Horizontal raster generator.

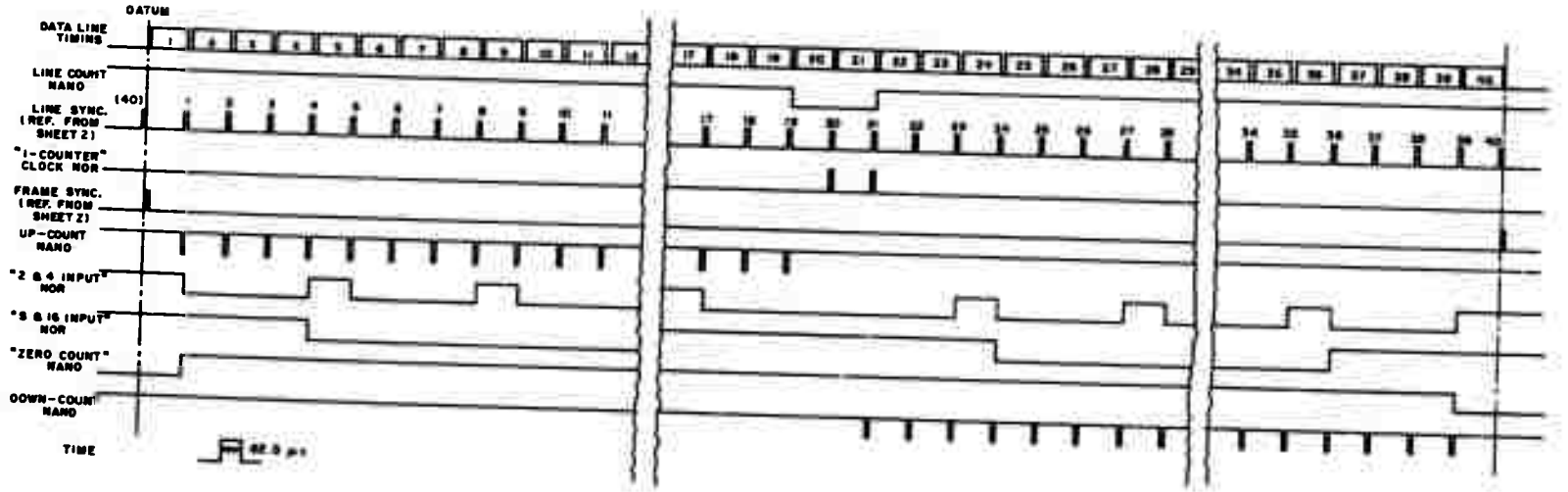


Fig. 55. Raster generator timing diagram. (cont.)
Sheet 3 - Horizontal gating waveforms.

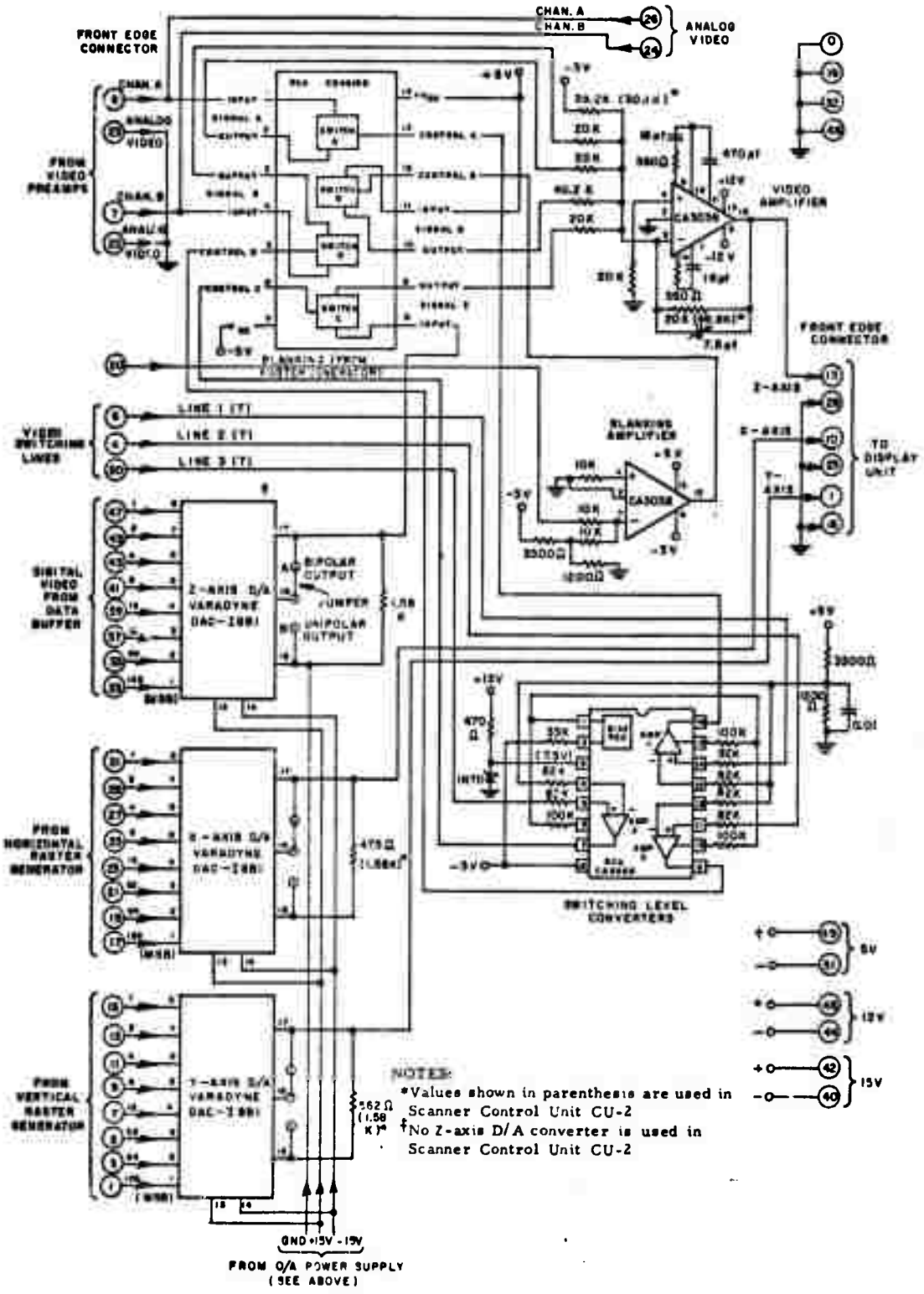


Fig. 56. Video switching and D/A converters logic diagram.

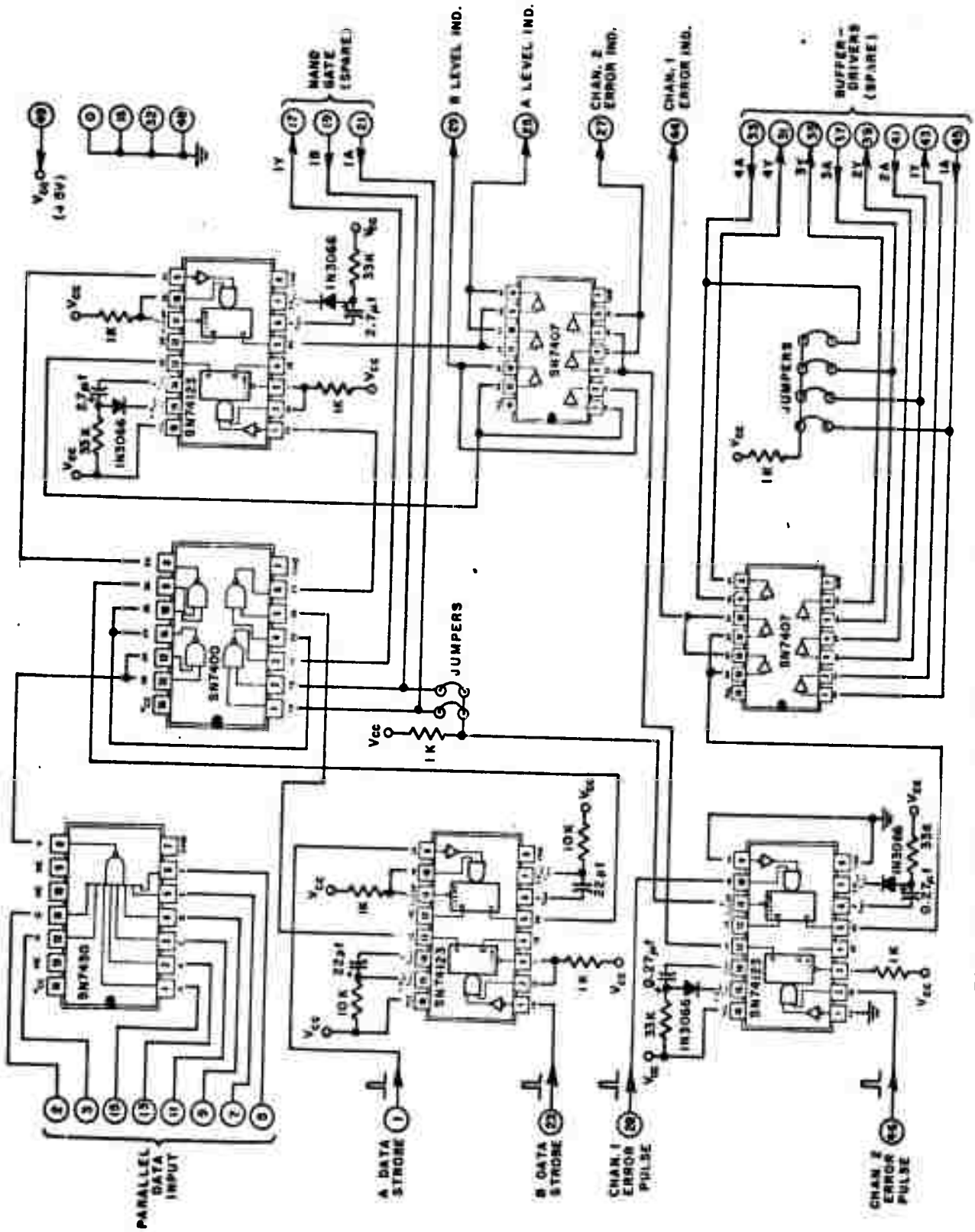


Fig. 57. Video level and error indicators logic diagram.

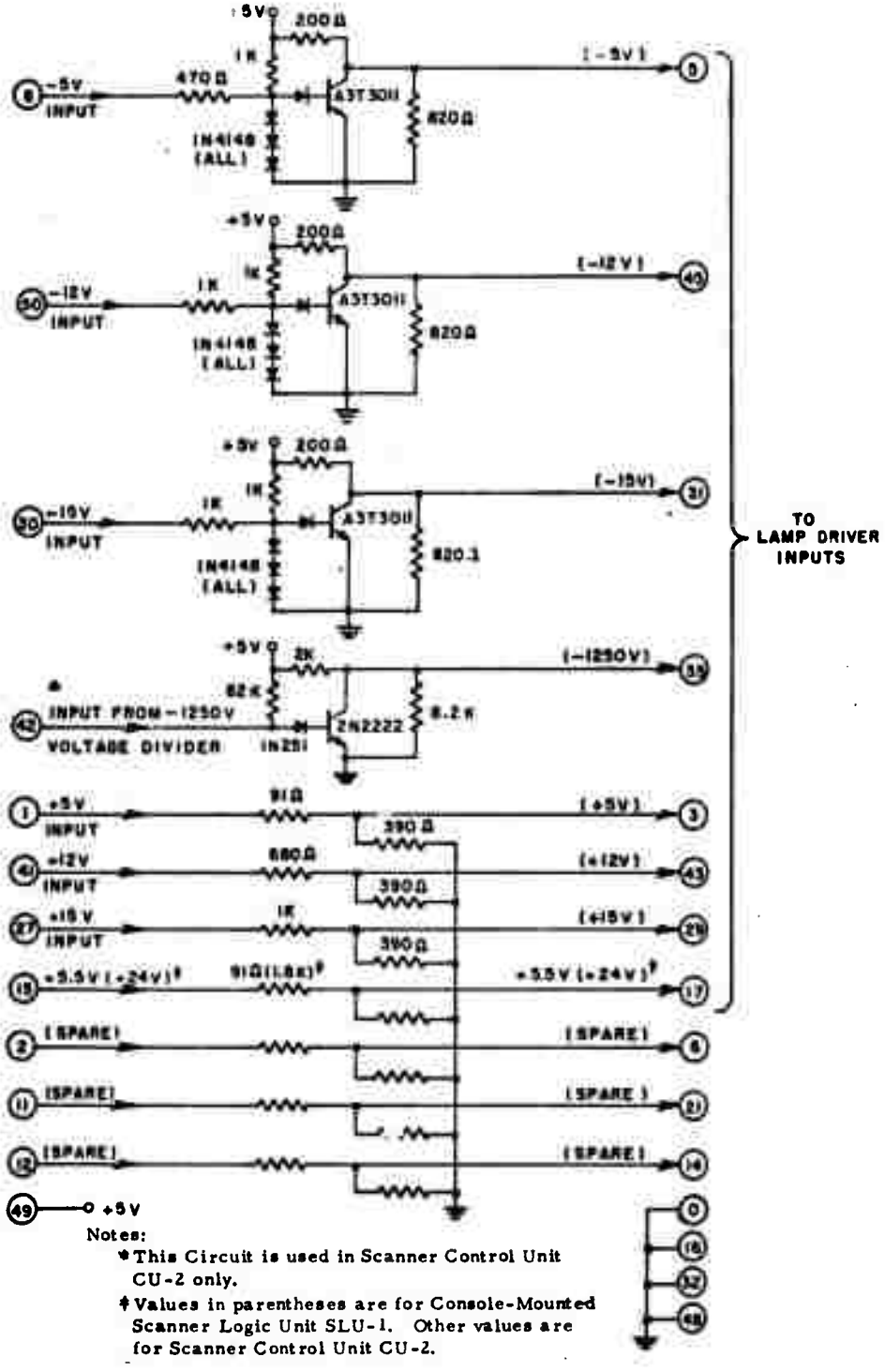


Fig. 58. Voltage dividers schmatic diagram.

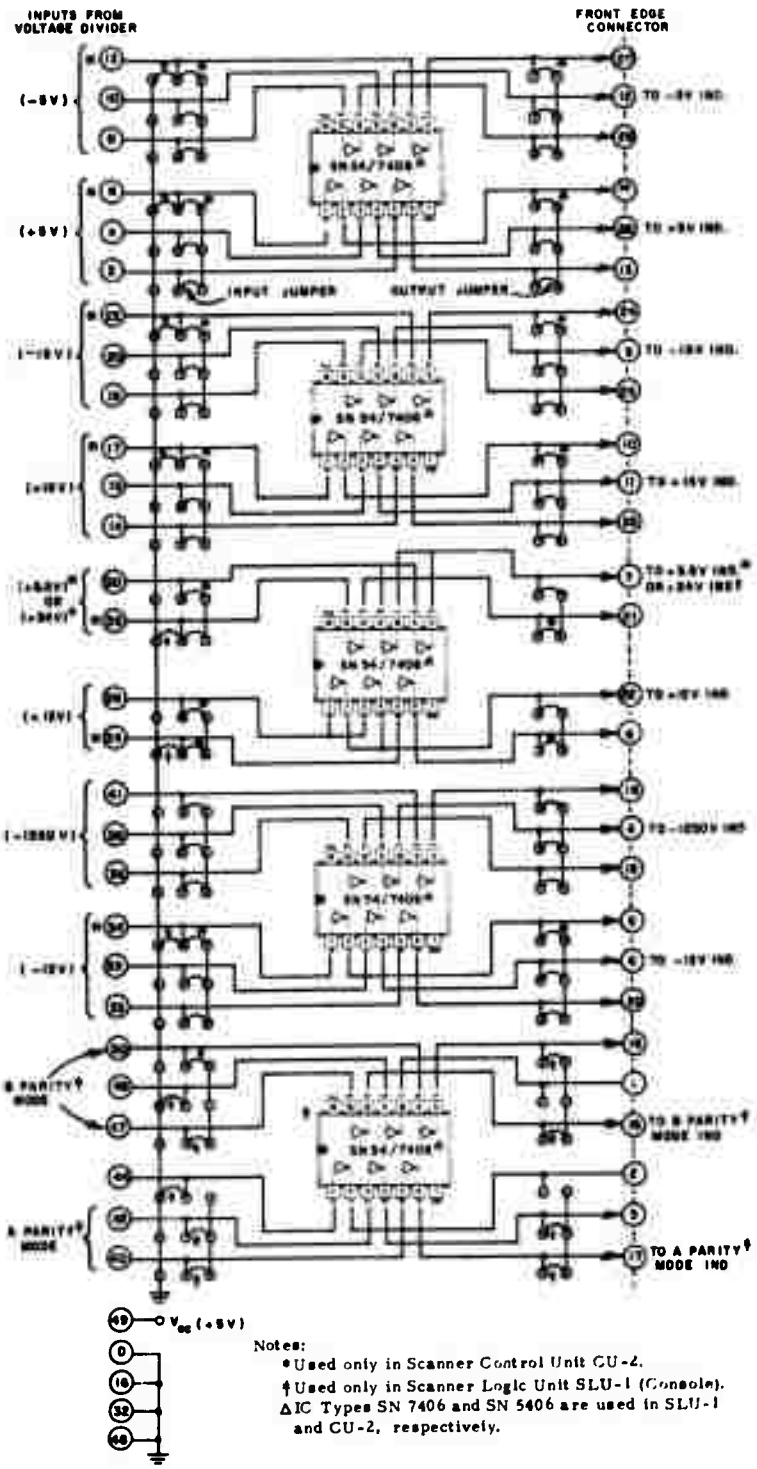


Fig. 59. Lamp drivers schematic diagram.

APPENDIX II - WORD SYNC AND RELATED PULSES REQUIRED FOR THE 2-CHANNEL IR SCANNER

This Appendix contains additional discussion of several waveforms generated by the B-sync generator (see Chap. IV, par. 9) which are required for 2-channel multiplexed operation.

Requirements:

1. Channel transfer pulses at the center of each data word to initiate sampling. These are obtained by ORing together Channel A and Channel B word sync pulses which occur at the center of each data space.

2. Raster word sync pulses for each channel which occur at (or near) the beginning of each data space. The Channel A and Channel B word sync pulses must be offset by approximately ½ data space to permit multiplexing and subsequent use of a single A/D converter.

3. A next channel address signal to program the multiplexer to sample the proper channel.

4. B-channel line sync must also be generated, lagging A-channel line sync by ½ data space.

Limitation:

1. The data spaces (times) and hence word length for each line of the image is different because an approximate rectangular image, rather than a pie shaped wedge, is being scanned by the scanning disc.

Method:

1. The B-channel image is made to lag the A-channel image by ½ the word length of the shortest (1st) line of the image via a rotation about the axis of the disk (approximately .004" at the radius of the 1st (outermost) scanning aperture).

2. Since the rotational speed of the disc is constant, rotation is proportional to time; hence each element of the B-channel image is delayed with respect to the corresponding element of the A-channel image by ½ the word length of the 1st (shortest) image line.

   This is illustrated by the timing diagrams of Fig. 60 in which:

   1. Only 6 elements (rather than the actual 40) per line are shown to illustrate the principles in minimum space, and

   2. Only the shortest (1st) and longest lines of the image are drawn (with arbitrary time scales and length ratio) to illustrate that lines of unequal length are accommodated.

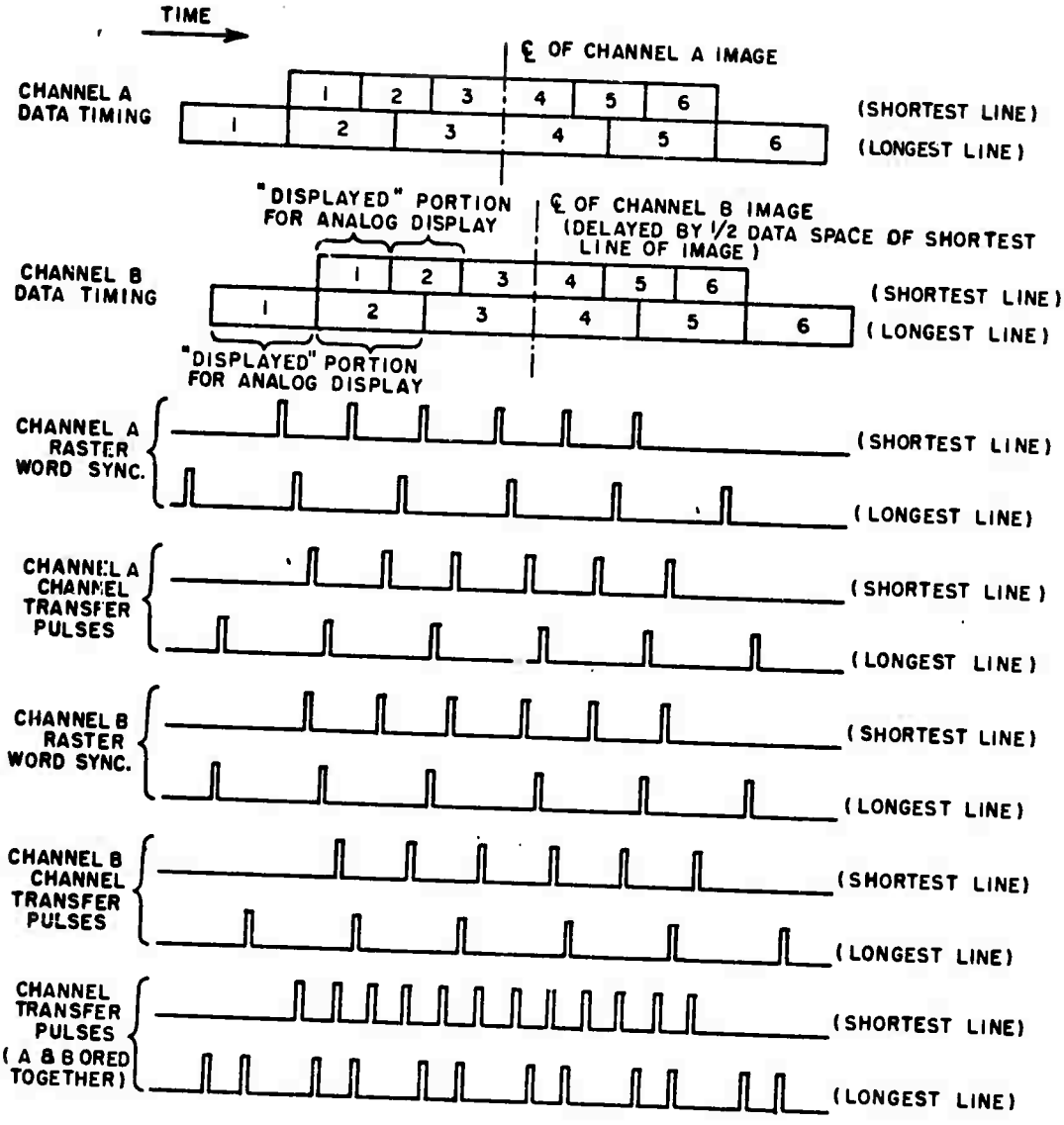


Fig. 60. Word sync related signals, timing diagram.

Since the Channel A raster word sync. pulses must occur 1st in time, these will be generated directly by the word sync. generator. They will:

1. Occur coincident with the start of each data space (word) for the shortest (1st) raster line, and will

2. Precede the center of each word space by the same amount for all data lines. (Thus if equal length samples are taken for all words used in an analog display, all such samples will be taken about the midpoint of each data word.)

The Channel A raster word sync. pulses thus defined are drawn next on the timing diagram.

The Channel A channel transfer pulses are next obtained from these generated pulses by means of a constant time delay equal to ½ the data space of the shortest line. (The actual delay gate timing used may be somewhat less than this to allow for propagation delays in the various circuits.) Note from the timing diagram that these then occur at the center of the data space, as required, for all words.

The B channel word sync. pulses could now be obtained from the corresponding A channel pulses via a constant time delay equal to ½ the data word space for the shortest line. These are next shown in the timing diagram. Note that the Channel B raster word sync. is (ideally) identical with the Channel A channel transfer pulses. However, propagation delays in the circuits for which these pulses are used will very likely differ, so that independent adjustment of the delays for these two pulse trains is desirable. Hence separate delay circuits are used to obtain these two signals. Channel B channel transfer pulses are then obtained from the Channel B raster word sync. pulses via an additional time delay (see the block diagram, Fig. 61).

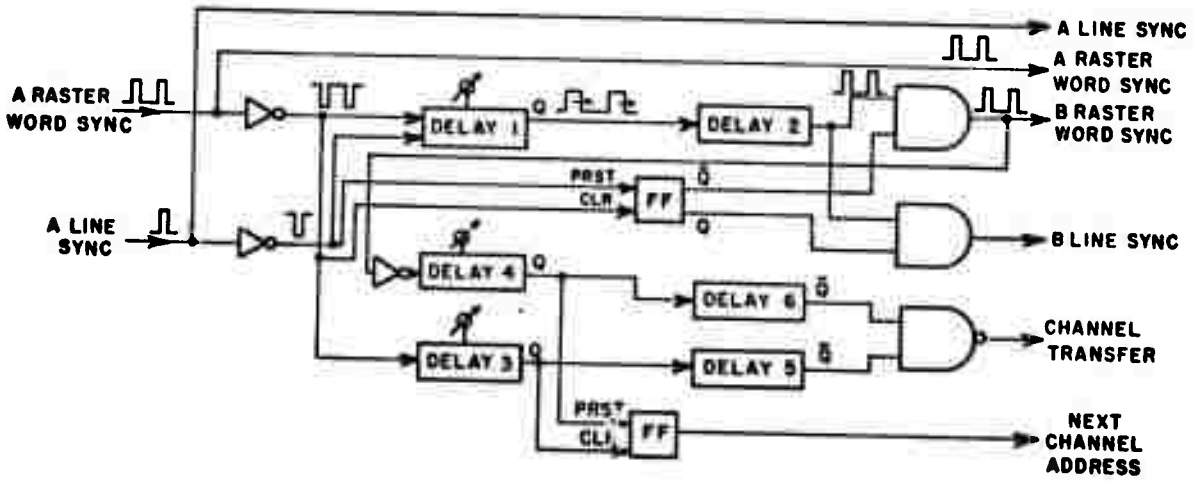


Fig. 61. Two-channel sync signal generation, block diagram.

The Channel A and Channel B channel transfer pulses are next ORed together for application to the multiplexer. This waveform is next shown in the timing diagram. The pulses are seen to be evenly spaced in the case of the shortest line but occur in pairs for the longest line, the minimum spacing being equal to that for the shortest line (i.e., ½ data word space of the shortest line). Thus, if the multiplexer and A/D converter is adequate for the shortest line, it will function properly for the longest line also even though sample spacing for this line might not at first glance appear optimum. (Note that it is not possible to first combine the A and B raster word sync pulses and then delay them via a single delay gate since a "100% duty cycle 1-shot" would be required - i.e., the required delay is approximately equal to the pulse spacing of the channel transfer wavetrain.)

A next channel address signal is now required to program the multiplexer to sample the proper channel. The proper address must be applied to the multiplexer prior to the arrival of the channel transfer pulse. This is accomplished by applying the delay gate outputs driven by the A-channel and B-channel raster word sync pulses to the clear and preset inputs, respectively, of a flip flip. The Q output of the flip flop is then used for the next channel address signal applied to the multiplexer.

A-channel line sync is directly generated and occurs ≈1½ data spaces (for the shortest line) ahead of the 1st A-channel raster word sync pulse. The B-channel line sync is obtained from the A-channel line sync via a delay equal to ½ data space for the shortest line. The same delay used for obtaining the B channel raster word sync is used, with a flip flop and gates for switching.

APPENDIX III - SCANNING DISC PARAMETERS AND SCANNING SEQUENCE

This appendix lists essential parameters of the scanning disc with respect to location of the scanning apertures and their use for image scanning and associated sync pulse generation. The physical layout of the disc relative to scanning hole numbers and image and sync reticle scanning positions is shown in Fig. 62. Table X lists the scanning, synchronization and display sequence, Table XI lists R-THETA coordinates of the scanning apertures and frame sync holes, while Table XII lists the scanning frequency (for the 40 data points) and lengths of the data space and dead space (see Fig. 63) for each image line.

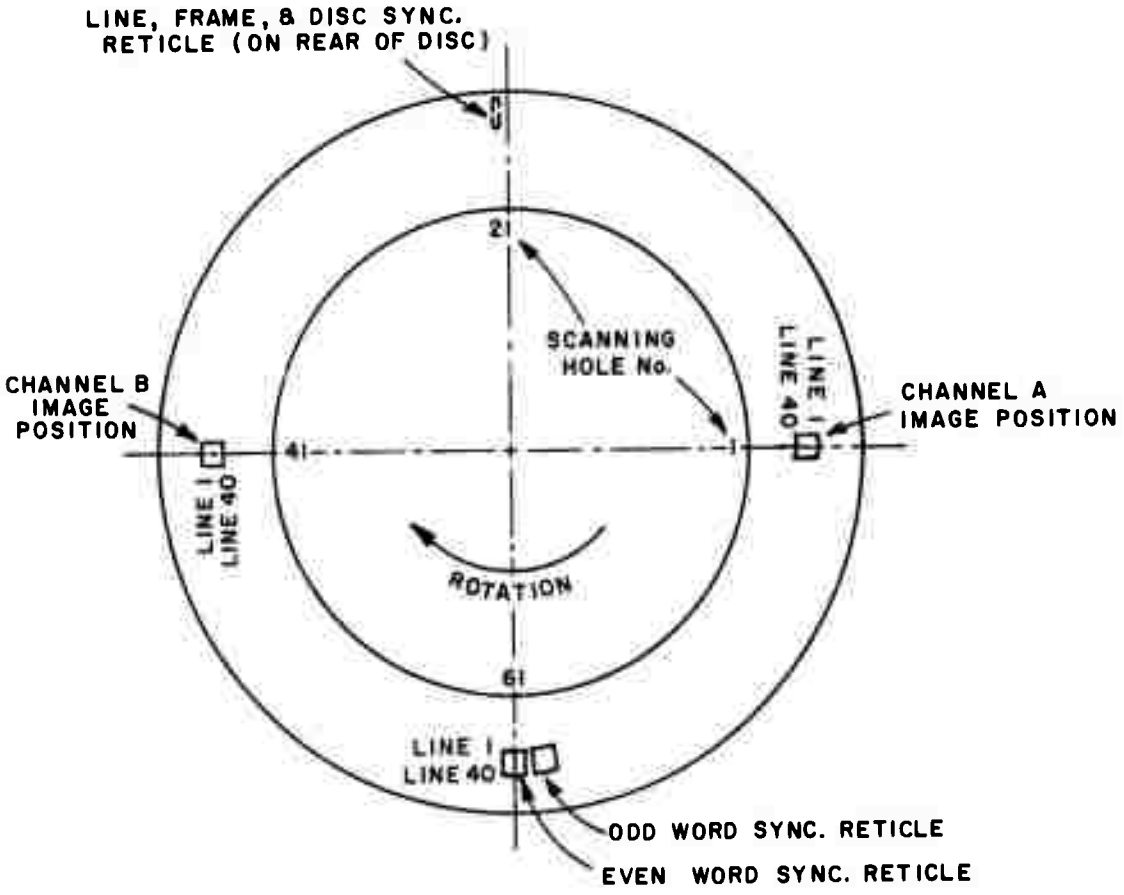


Fig. 62. Scanning disc, front view.

TABLE X
SCANNING, SYNCHRONIZATION, AND DISPLAY SEQUENCE

Frame & Disc Sync →	A-Image Scanning Hole	B-Image Scanning Hole	Raster Line No. Time Sequence	Raster Line No. Line Position	Word Sync Hole No. Odd	Word Sync Hole No. Even	Reticle Line (Top-Bottom) Odd	Reticle Line (Top-Bottom) Even	← Frame & Disc Sync
	1	41	1	1	62	61	3	1	
	2	42	2	3	63	62	5	3	
	3	43	3	5	64	63	7	5	
	4	44	4	7	65	64	9	7	
	5	45	5	9	66	65	11	9	
	6	46	6	11	67	66	13	11	
	7	47	7	13	68	67	15	13	
	8	48	8	15	69	68	17	15	
	9	49	9	17	70	69	19	17	
	10	50	10	19	71	70	21	19	
	11	51	11	21	72	71	23	21	
	12	52	12	23	73	72	25	23	
	13	53	13	25	74	73	27	25	
	14	54	14	27	75	74	29	27	
	15	55	15	29	76	75	31	29	
	16	56	16	31	77	76	33	31	
	17	57	17	33	78	77	35	33	
	18	58	18	35	79	78	37	35	
	19	59	19	37	80	79	39	37	
	20	60	20	39	1	80	40	39	
	21	61	21	40	2	1	38	40	
	22	62	22	38	3	2	36	38	
	23	63	23	36	4	3	34	36	
	24	64	24	34	5	4	32	34	
	25	65	25	32	6	5	30	32	
	26	66	26	30	7	6	28	30	

TABLE X (Continued)

A-Image Scanning Hole	B-Image Scanning Hole	Raster Line No. Time Sequence	Raster Line No. Line Position	Word Sync Hole No. Odd	Word Sync Hole No. Even	Reticle Line (Top-Bottom) Odd	Reticle Line (Top-Bottom) Even
27	67	27	28	8	7	26	28
28	68	28	26	9	8	24	26
29	69	29	24	10	9	22	24
30	70	30	22	11	10	20	22
31	71	31	20	12	11	18	20
32	72	32	18	13	12	16	18
33	73	33	16	14	13	14	16
34	74	34	14	15	14	12	14
35	75	35	12	16	15	10	12
36	76	36	10	17	16	8	10
37	77	37	8	18	17	6	8
38	78	38	6	19	18	4	6
39	79	39	4	20	19	2	4
40	80	40	2	21	20	1	2
41	1	41	1	22	21	3	1
42	2	42	3	23	22	5	3
43	3	43	5	24	23	7	5
44	4	44	7	25	24	9	7
45	5	45	9	26	25	11	9
46	6	46	11	27	26	13	11
47	7	47	13	28	27	15	13
48	8	48	15	29	28	17	15
49	9	49	17	30	29	19	17
50	10	50	19	31	30	21	19
51	11	51	21	32	31	23	21
52	12	52	23	33	32	25	23
53	13	53	25	34	33	27	25
54	14	54	27	35	34	29	27
55	15	55	29	36	35	31	29

Frame Sync →

← Frame Sync

TABLE X (Continued)

A-Image Scanning Hole	B-Image Scanning Hole	Raster Line No.		Word Sync Hole No.		Reticle Line (Top-Bottom)	
		Time Sequence	Line Position	Odd	Even	Odd	Even
56	16	56	31	37	36	33	31
57	17	57	33	38	37	35	33
58	18	58	35	39	38	37	35
59	19	59	37	40	39	39	37
60	20	60	39	41	40	40	39
61	21	61	40	42	41	38	40
62	22	62	38	43	42	36	38
63	23	63	36	44	43	34	36
64	24	64	34	45	44	32	34
65	25	65	32	46	45	30	32
66	26	66	30	47	46	28	30
67	27	67	28	48	47	26	28
68	28	68	26	49	48	24	26
69	29	69	24	50	49	22	24
70	30	70	22	51	50	20	22
71	31	71	20	52	51	18	20
72	32	72	18	53	52	16	18
73	33	73	16	54	53	14	16
74	34	74	14	55	54	12	14
75	35	75	12	56	55	10	12
76	36	76	10	57	56	8	10
77	37	77	8	58	57	6	8
78	38	78	6	59	58	4	6
79	39	79	4	60	59	2	4
80	40	80	2	61	60	1	2

TABLE XI
R-THETA COORDINATES OF THE SCANNING DISC APERTURES

Hole No.	Theta Degrees	Theta Deg.	Theta Min.	Theta Sec.	R In.
1	0.0	0	0	0.	4.52521
2	4.50000	4	30	0.	4.50946
3	9.00000	9	0	0.	4.49371
4	13.50000	13	30	0.	4.47796
5	18.00000	18	0	0.	4.46221
6	22.50000	22	30	0.	4.44647
7	27.00000	27	0	0.	4.43072
8	31.50000	31	30	0.	4.41497
9	36.00000	36	0	0.	4.39922
10	40.50000	40	30	0.	4.38347
11	45.00000	45	0	0.	4.36773
12	49.50000	49	30	0.	4.35198
13	54.00000	54	0	0.	4.33623
14	58.50000	58	30	0.	4.32048
15	63.00000	63	0	0.	4.30473
16	67.50000	67	30	0.	4.28899
17	72.00000	72	0	0.	4.27324
18	76.50000	76	30	0.	4.25749
19	81.00000	81	0	0.	4.24174
20	85.50000	85	30	0.	4.22599
21	90.00000	90	0	0.	4.21812
22	94.50000	94	30	0.	4.23387
23	99.00000	99	0	0.	4.24962
24	103.50000	103	30	0.	4.26536
25	108.00000	108	0	0.	4.28111
26	112.50000	112	30	0.	4.29686
27	117.00000	117	0	0.	4.31261
28	121.50000	121	30	0.	4.32836
29	126.00000	126	0	0.	4.34410
30	130.50000	130	30	0.	4.35985
31	135.00000	135	0	0.	4.37560
32	139.50000	139	30	0.	4.39135
33	144.00000	144	0	0.	4.40710
34	148.50000	148	30	0.	4.42284
35	153.00000	153	0	0.	4.43859
36	157.50000	157	30	0.	4.45434
37	162.00000	162	0	0.	4.47009
38	166.50000	166	30	0.	4.48584
39	171.00000	171	0	0.	4.50158
40	175.50000	175	30	0.	4.51733
41	-180.00000	180	0	0.	4.52521
42	-175.50000	184	30	0.	4.50946
43	-171.00000	189	0	0.	4.49371
44	-166.50000	193	30	0.	4.47796
45	-162.00000	198	0	0.	4.46221
46	-157.50000	202	30	0.	4.44647
47	-153.00000	207	0	0.	4.43072

Tolerances

Radius ±2.5/10,000 inch

Theta ±3/1,000 degree

≈ ±10 seconds

TABLE XI (Continued)

Hole No.	Theta Degrees	Theta Deg.	Theta Min.	Theta Sec.	R In.	
48	-148.50000	211	30	0.	4.41497	
49	-144.00000	216	0	0.	4.39922	
50	-139.50000	220	30	0.	4.38347	
51	-135.00000	225	0	0.	4.36773	
52	-130.50000	229	30	0.	4.35198	
53	-126.00000	234	0	0.	4.33623	
54	-121.50000	238	30	0.	4.32048	
55	-117.00000	243	0	0.	4.30473	
56	-112.50000	247	30	0.	4.28899	
57	-108.00000	252	0	0.	4.27324	
58	-103.50000	256	30	0.	4.25749	
59	- 99.00000	261	0	0.	4.24174	
60	- 94.50000	265	30	0.	4.22599	
61	- 90.00000	270	0	0.	4.21812	
62	- 85.50000	274	30	0.	4.23387	
63	- 81.00000	279	0	0.	4.24962	
64	- 76.50000	283	30	0.	4.26536	
65	- 72.00000	288	0	0.	4.28111	
66	- 67.50000	292	30	0.	4.29686	
67	- 63.00000	297	0	0.	4.31261	
68	- 58.50000	301	30	0.	4.32836	
69	- 54.00000	306	0	0.	4.34410	
70	- 49.50000	310	30	0.	4.35985	
71	- 45.00000	315	0	0.	4.37560	
72	- 40.50000	319	30	0.	4.39135	
73	- 36.00000	324	0	0.	4.40710	
74	- 31.50000	328	30	0.	4.42284	
75	- 27.00000	333	0	0.	4.43859	
76	- 22.50000	337	30	0.	4.45434	
77	- 18.00000	342	0	0.	4.47009	
78	- 13.50000	346	30	0.	4.48584	
79	- 9.00000	351	0	0.	4.50158	
80	- 4.50000	355	30	0.	4.51733	
81	- 90.50000	269	30	0.	4.75000	Frame Sync Holes
82	89.50000	89	30	0.	4.75000	
83	89.50000	89	30	0.	4.65000	Disc Sync Hole

TABLE XII
DISC TIMING INFORMATION

N	Dead Space/2 (USEC)	Data Space (USEC)	Frequency (I/SEC)	DS(N)/2+DS(N+1)/2 (USEC)	DS(N)/2+DS(N-1)/2 (USEC)
1	8.5016	107.9968	361121.753	16.8147	16.9091
2	8.3131	108.3738	359865.626	16.4364	16.8147
3	8.1233	108.7534	358609.501	16.0555	16.4364
4	7.9322	109.1357	357353.381	15.6718	16.0555
5	7.7397	109.5206	356097.264	15.2855	15.6718
6	7.5458	109.9083	354841.150	14.8964	15.2855
7	7.3506	110.2988	353585.041	14.5046	14.8964
8	7.1540	110.6920	352328.935	14.1100	14.5046
9	6.9560	111.0881	351072.833	13.7125	14.1100
10	6.7565	111.4869	349816.734	13.3122	13.7125
11	6.5556	111.8887	348560.640	12.9090	13.3122
12	6.3533	112.2934	347304.550	12.5028	12.9090
13	6.1495	112.7010	346048.463	12.0937	12.5028
14	5.9442	113.1115	344792.381	11.6817	12.0937
15	5.7374	113.5251	343536.302	11.2666	11.6817
16	5.5291	113.9417	342280.228	10.8484	11.2666
17	5.3193	114.3614	341024.158	10.4272	10.8484
18	5.1079	114.7842	339768.092	10.0029	10.4272
19	4.8950	115.2101	338512.030	9.5754	10.0029
20	4.6804	115.6392	337255.972	9.2530	9.5754
21	4.5725	115.8549	336627.945	9.7895	9.3604
22	4.7879	115.4242	337884.001	9.7895	9.3604
23	5.0016	114.9967	339140.060	10.2154	9.7895
24	5.2138	114.5724	340396.124	10.6382	10.2154
25	5.4244	114.1512	341652.192	11.0579	10.6382
26	5.6335	113.7330	342908.264	11.4745	11.0579
27	5.8410	113.3180	344164.341	11.8881	11.4745
28	6.0471	112.9059	345420.421	12.2987	11.8881

TABLE XII (Continued)

N	Dead Space/2 (USEC)	Data Space (USEC)	Frequency (I/SEC)	DS(N)/2+DS(N+1)/2 (USEC)	DS(N)/2+DS(N-1)/2 (USEC)
29	6.2516	112.4968	346676.506	12.7063	12.2987
30	6.4547	112.0907	347932.594	13.1109	12.7063
31	6.6563	111.6875	349188.687	13.5127	13.1109
32	6.8564	111.2871	350444.783	13.9116	13.5127
33	7.0552	110.8897	351700.883	14.3076	13.9116
34	7.2525	110.4951	352956.987	14.7009	14.3076
35	7.4484	110.1032	354213.095	15.0913	14.7009
36	7.6429	109.7141	355469.206	15.4790	15.0913
37	7.8361	109.3278	356725.322	15.8640	15.4790
38	8.0279	108.9442	357981.441	16.2463	15.8640
39	8.2184	108.5633	359237.563	16.6259	16.2463
40	8.4075	108.1850	360493.689	16.9091	16.6259
41	8.5016	107.9968	361121.753	16.8147	16.9091
42	8.3131	108.3738	359865.626	16.4364	16.8147
43	8.1233	108.7534	358609.501	16.0555	16.4364
44	7.9322	109.1357	357353.381	15.6718	16.0555
45	7.7397	109.5206	356097.264	15.2855	15.6718
46	7.5458	109.9083	354841.150	14.8964	15.2855
47	7.3506	110.2988	353585.041	14.5046	14.8964
48	7.1540	110.6920	352328.935	14.1100	14.5046
49	6.9560	111.0881	351072.833	13.7125	14.1100
50	6.7565	111.4869	349816.734	13.3122	13.7125
51	6.5556	111.8887	348560.640	12.9090	13.3122
52	6.3533	112.2934	347304.550	12.5028	12.9090
53	6.1495	112.7010	346048.463	12.0937	12.5028
54	5.9442	113.1115	344792.381	11.6817	12.0937
55	5.7374	113.5251	343536.302	11.2666	11.6817
56	5.5291	113.9417	342280.228	10.8484	11.2666
57	5.3193	114.3614	341024.158	10.4272	10.8484
58	5.1079	114.7842	339768.092	10.0029	10.4272

TABLE XII (Continued)

N	Dead Space/2 (USEC)	Data Space (USEC)	Frequency (I/SEC)	DS(N)/2+DS(N+1)/2 (USEC)	DS(N)/2+DS(N-1)/2 (USEC)
59	4.8950	115.2101	338512.030	9.5754	10.0029
60	4.6804	115.6392	337255.972	9.2530	9.5754
61	4.5725	115.8549	336627.945	9.3604	9.2530
62	4.7879	115.4242	337884.001	9.7895	9.3604
63	5.0016	114.9967	339140.060	10.2154	9.7895
64	5.2138	114.5724	340396.124	10.6382	10.2154
65	5.4244	114.1512	341652.192	11.0579	10.6382
66	5.6335	113.7330	342908.264	11.4745	11.0579
67	5.8410	113.3180	344164.341	11.8881	11.4745
68	6.0471	112.9059	345420.421	12.2987	11.8881
69	6.2516	112.4968	346676.506	12.7063	12.2987
70	6.4547	112.0907	347932.594	13.1109	12.7063
71	6.6563	111.6875	349188.687	13.5127	13.1109
72	6.8564	111.2871	350444.783	13.9116	13.5127
73	7.0552	110.8897	351700.883	14.3076	13.9116
74	7.2525	110.4951	352956.987	14.7009	14.3076
75	7.4484	110.1032	354213.095	15.0913	14.7009
76	7.6429	109.7141	355469.206	15.4790	15.0913
77	7.8361	109.3278	356725.322	15.8640	15.4790
78	8.0279	108.9442	357981.441	16.2463	15.8640
79	8.2184	108.5633	359237.563	16.6259	16.2463
80	8.4075	108.1850	360493.689	16.9091	16.6259

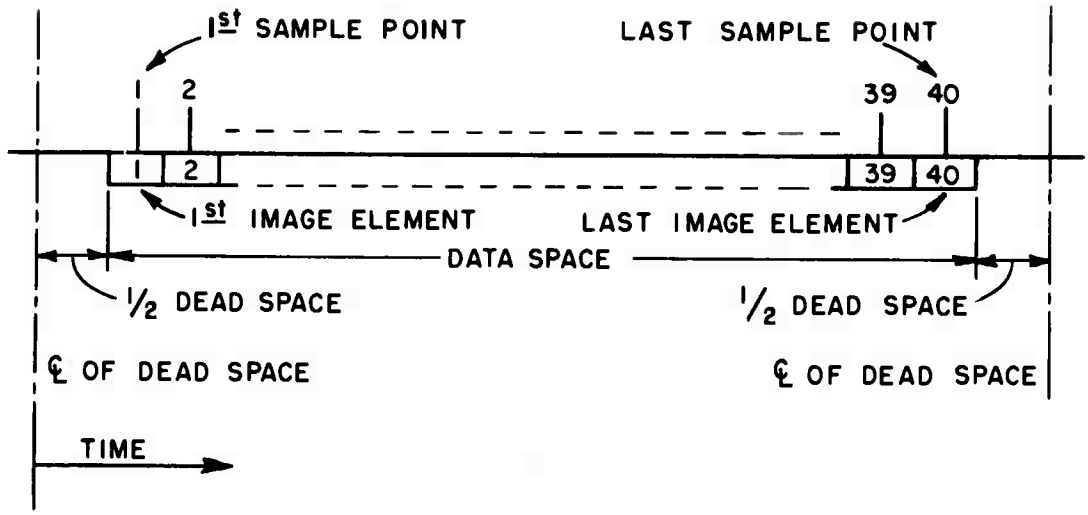


Fig. 63. Scanning line format.

APPENDIX IV - IR SCANNER ALIGNMENT AND MAINTENANCE

A. General Maintenance Procedures

Both mechanical and electrical components of the IR scanner system are quite stable and re-alignment should not normally be required except perhaps after component replacement following accidental damage or failure. No periodic maintenance of the scanner and console components is required other than keeping the system clean and occasionally drying the nitrogen filters if erratic detector cooling is experienced (see instructions for regeneration printed on the body of the filters). The magnetic tape recorder does require periodic maintenance, however, and the manufacturer's manuals[8,9] should be consulted and the maintenance instructions followed (see also Chapter III, Section B-2-c, of this report).

The gold-coated IR imaging optics should only be cleaned using an air blast since these optical coatings are very easily damaged. Lens tissue, and a drop of cleaning solution may be used if necessary on the various sync system lenses, and, with extreme care to avoid scratching, on the first surface mirrors used in the word sync system, if necessary.

The scanning disc apertures may be cleaned by an air blast, using solvent if necessary, or in an extreme case not yielding to this treatment, a 0.008 in. dia. drill may be used - very lightly held in the fingers, and very carefully used to avoid enlarging the aperture.

In the event of system malfunction and, in any case, prior to attempting any alignment procedures given below, the following should first be checked:

1. Power Supplies:

   a. Make sure that all power supply indicators are lit. If not, turn power off and then back-on to reset any crowbar circuits which may have tripped because of a temporary voltage or current overload. (Note an off cycle of 60 seconds may be required to thus reset the +5.5 v supply.) If this fails, check indicator lamps, power supply fuses and other components to determine cause of failure, and replace, as required.

   b. If malfunction presists, and before any alignment procedures are attempted, check all associated power supply voltages with an accurate voltmeter (digital voltmeter with millivolt sensitivity preferred) and readjust, if required. Care must be used not to set the low voltage regulated logic supplies more than ½ volt above nominal, even temporarily, or logic components may be damaged. It is recommended that the loads be disconnected prior to adjusting these supplies, but the voltage should then be rechecked with normal load applied.

Crowbar circuits, where used, are to be set ½ volt higher than the nominal output voltage. WARNING: All logic circuits must be disconnected from the power supply to prevent damage prior to attempting a crowbar circuit adjustment.

2. Scanning Disc and Sync System:

   a. Make sure that both sync projector lamps are lit. If not, check +5.5 volt power supply as above or replace sync projector lamps as required (see below).

   b. Make sure all scanning and sync apertures of the scanning disc are clear. (See above for cleaning procedure.) This may be checked if necessary by observing the signal output of each sync detector (at the sync detector output connector - see Figs. 15 and 17) via an oscilloscope.

      Eighty output pulse trains (20 pulses per train) corresponding to 80 successive data lines should be viewed (i.e., 1 complete rotation of the scanning disc). This can best be done by syncing the A-sweep of the oscilloscope with the disc sync output (available on TP5 of the scanner control unit card cage - see Fig. 18) and viewing each successive pulse group by means of the delayed sweep.

      If one or more pulse groups are found to be of significantly lower amplitude than the others, the corresponding scanning disc aperture is probably partly obstructed and should be cleared. The information contained in Table X of Appendix III will aid in determining a specific aperture which requires cleaning from the observed pulse trains.

   c. Spots of dirt on the sync system 1st surface mirrors or projector reticles could also cause individual pulses to drop out, but would normally not reduce the amplitude of an entire pulse train as would an obstructed aperture. The possibility of this condition existing can also be checked, as above, and should be corrected if required.

3. Scanner Motor Speed:

   For proper system operation scanner motor speed must be correct to within approximately ±5%. Low line voltage (400 Hz 3-phase supply) may cause the motor to operate below synchronous speed. The line-to-neutral voltage, at the motor, for each phase of the supply should not be less than 117 volts to insure proper operation.

   Motor speed may easily be checked for synchronous operation as follows: With IR detectors warm, video gain

full on, and the remainder of the system in normal operation, a certain amount of 400 Hz hum modulation (i.e., variation of intensity with horizontal position) will be observable on the visual display raster pattern. This is produced by magnetic coupling from the scanner motor windings to the IR detectors. If this pattern is stationary, and does not exhibit a slow drift with time, the scanner motor speed is synchronous with the 400 Hz power line frequency.

B. Sync Projector Lamp Replacement

The procedure for replacing a defective sync projector lamp is as follows:

1. Slide back plastic boot covering lamp base to expose connections
2. Unsolder wires from lamp base.
3. Remove 3 8-32 socket head cap screws holding lamp mounting plate to projector and remove lamp and plate.
4. Loosen 3 6-32 socket head set screws in rim of mounting plate and remove defective lamp.
5. Install new lamp (Philips Type 13347W, 6 volt-15 watt) by reversing the above procedure. Tighten set screws (step 4) just sufficient to hold lamp firmly. Excess tightening will damage lamp. Tighten the socket head cap screws (step 3), each fitted with a flat washer and spring lock washer, only enough to hold lamp mounting plate in position.
6. Adjust lamp position for even illumination of the reticle as follows: turn system power on and observe raster pattern on the console visual display indicator using the SERIAL IN position of the video selector switch (this position is most sensitive to alignment errors). Slide the lamp mounting plate to the limits of its travel (the mounting holes are larger than the mounting screws) while watching the raster display to determine the midpoint, both vertically and horizontally, of lamp positions which result in a proper raster display. Set lamp mounting plate to this position and tighten the 3 8-32 socket head mounting screws.

6a. If the above adjustment procedure (step 6) cannot be used (i.e., locations are such that the console indicator cannot be seen from the scanner location) then the output of the associated sync detector should be viewed on an oscilloscope as in paragraph A-2-b, above, and the sync projector lamp should be adjusted to obtain the most uniform amplitude distribution of detector output pulses.

C. System Alignment Procedures

Before system alignment is attempted, perform all preliminary tests indicated in Section A above. It is further recommended that, prior to performing an alignment procedure, the need for that particular alignment should be verified by appropriate oscilloscope checks of the various waveforms. When comparing the various waveforms obtained with the timing

diagrams of Appendix I, remember that these diagrams in general represent ideal waveforms, times are nominal, and the various propagation delays of the logic elements are not included; hence the observed wave shapes may differ from these to some extent, yet still be correct.

1. Final Alignment - General Procedure

The final criterion for proper system alignment is proper system operation with maximum deviation permitted before improper operation occurs. Hence, with the system nominally aligned and operating properly, or nearly so, final adjustment of most alignment controls can be performed as follows:

a. With system power on (detector cooling not required) set the console display indicators to the SERIAL IN position and observe the raster pattern. Since some adjustments affect the two channels differently, both A and B channels should be observed. (If two indicators are installed, switch one to each channel; otherwise switch periodically as required to observe both channels.)

b. Note the initial setting of the adjustment to be attempted so that it can be returned to its original position, if required.

c. While observing the raster patterns vary the adjustment in each direction and determine the limits over which proper operation can be obtained.

d. If definite limits are found in step c, set the adjustment to the midpoint of the range of proper operation.

e. If such limits are not found, return the adjustment to its original setting as determined in step b, above.

The above procedure should prove adequate for nearly all field alignment requirements unless system modifications are made, the system is seriously damaged, or catastrophic failures requiring major component replacement occur. In such a case the following alignment procedures may be required. The scanner must be in operation (detectors uncooled) during alignment.

2. Scanner Sync Generator Alignment

a. Set the odd word sync and even word sync high voltage pots accessible on the front plate of the scanner (Fig. 10) fully clockwise.

b. Using an oscilloscope with delayed sweep and dual trace capability observe the outputs of the two word sync detectors at their respective BNC output connectors. Oscilloscope sync for this, and all following procedures, should be obtained using the disc sync output, TP5 of the scanner control unit card cage (Fig. 18).

c. Signal amplitudes should be approximately 350 millivolts. If the two waveshapes are not of approximately equal amplitudes reduce the higher one by turning the corresponding pot counterclockwise.

d. View the output of the line, frame, and disc sync detector on the oscilloscope as above. Since the disc sync pulse occurs last in the pulse train it will be necessary to use delayed sweep to observe the line, frame, and disc sync pulses simultaneously. Adjust the line, frame, and disc sync high voltage pot (Fig. 18) for approximately 350 millivolts peak amplitude of the lowest of the three pulses.

e. Note the positions of all 3 high voltage controls so they may be reset to these positions after the remaining steps have been performed.

f. Trigger level adjustments are now performed. The controls are located on the scanner sync generator board, slot 12 of the scanner control unit card cage. Control locations are given in Fig. 64.

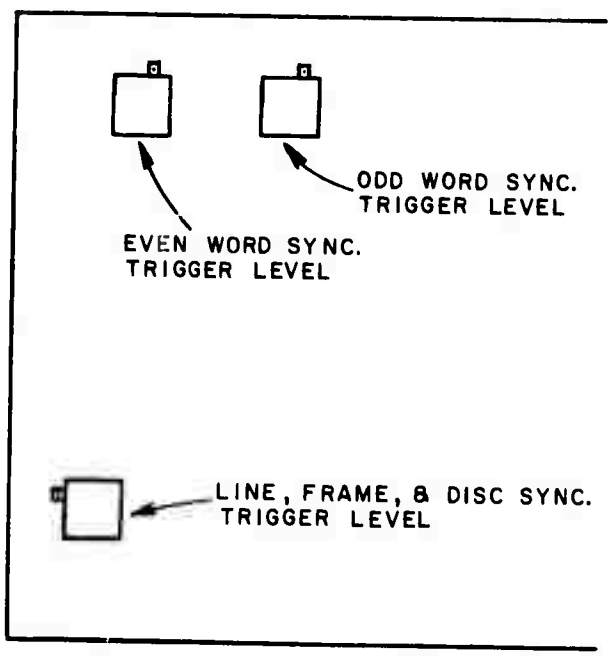


Fig. 64. Scanner sync generator control locations.

g. Using disc sync (TP5) as above, view the following waveshapes on the oscilloscope:

   (1) odd word sync detector output (use a co-ax tee so that detector is still connected to scanner control unit).
   (2) A raster word sync, TP 2 on card cage.

h. Choose level on wave shape (1) at which triggering is desired. This should be approximately midpoint on the negative-going leading edge of each pulse, and must be chosen for reliable triggering from the lowest sync pulses, but significantly greater than the noise level.

i. After noting original position so that it may be reset, turn odd word sync high voltage pot ccw to reduce peaks of waveform (1) to the value chosen in step h.

j. Set the odd word sync trigger level pot (Fig. 64) so that triggering just occurs as shown by waveshape (2). (NOTE: since this waveshape normally contains both even and odd word sync pulses it is helpful to remove the signal or h.v. cable from the detector not currently in use so that only the desired pulses are present.)

k. Return the high voltage pot (step i) to its original setting

l. Repeat g through k above for even word sync. Waveshape (1) will now be obtained from the even word sync detector.

m. Repeat g through k above for line, frame, and disc sync. Waveshape (1) will now be obtained from the line, frame, and disc sync detector. Waveshape (2) is taken from TP1 of the card cage.

NOTE: With detector connected to the scanner sync generator, a break in slope occurs at the trigger point in waveshape (1) as shown in Fig. 65.

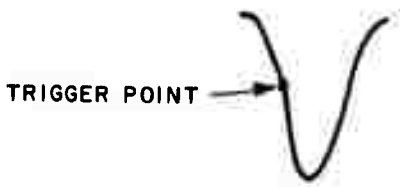


Fig. 65. Sync detector waveform.

3. Sync Separator Alignment

Two identical sync separators are used, one located in slot 11 of the scanner control unit card cage, and the other in the scanner logic unit (console card cage), slot 5. Control locations are given in Fig. 66. Alignment consists of adjusting the timing of the various delay gates. Gate timing is determined by oscilloscope measurement at the Q output of the corresponding gate (see Fig. 39). An extender board may be used so that the required points on the card are accessible, or test leads may be temporarily soldered onto the board for this purpose.

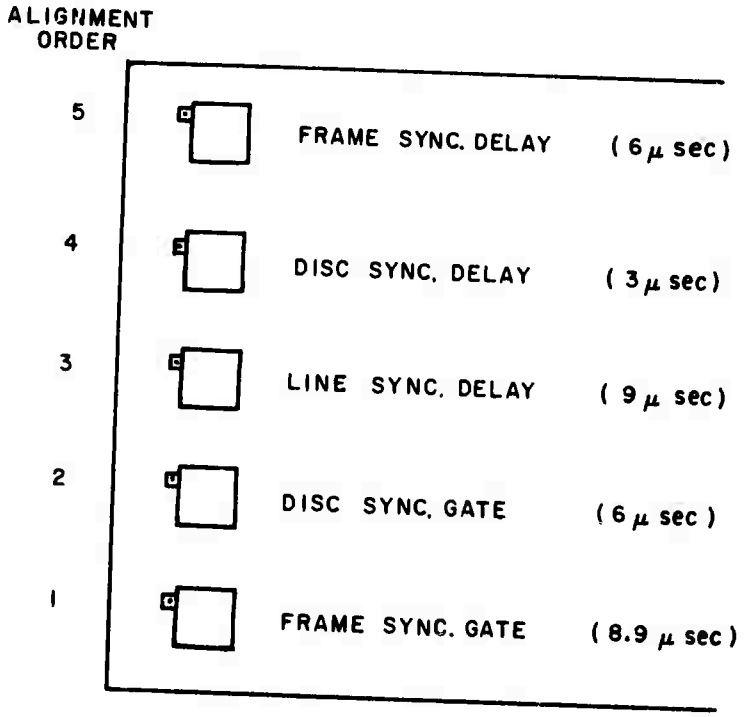


Fig. 66. Sync separator control locations.

a. Adjust all delay gates to obtain the delay times indicated in Fig. 66. Adjustments should be performed in the order indicated on this figure.

b. After alignment of the line, frame, and disc sync projector has been performed (see paragraph 6 below). The line and frame sync delays may be readjusted slightly, if desired, to obtain the relative timing (3 μs between pulses) between line, frame, and disc sync pulses shown in Fig. 40. These pulses are available at TP3, TP4, and TP5 of the scanner control unit card cage, respectively, for the scanner board; and from card connector pins 5-39, 5-23, and 5-7, respectively, for the console-mounted board.

4. B-sync Generator Alignment

Two identical units are used, one located in the scanner control unit card cage, slot 10, and the other in the scanner logic unit, slot 6. Control locations are given in Fig. 67.

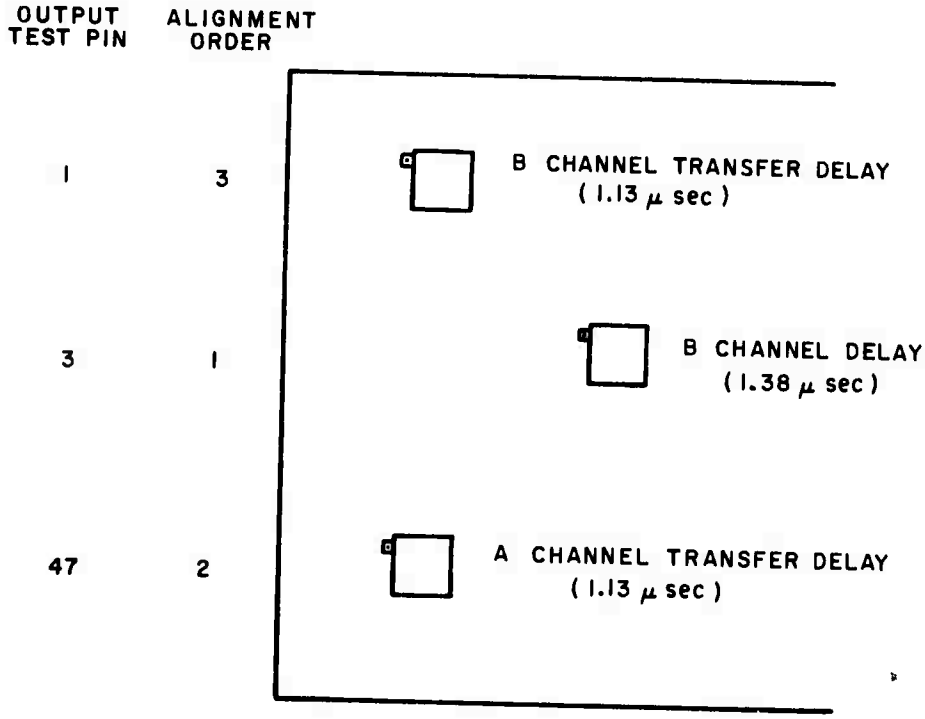


Fig. 67. B-sync generator control locations.

a. Adjust the 3 delay gates, in the specified order, to obtain the delay times indicated. The required test waveforms are available at the circuit board pins indicated (see Fig. 67).

b. Final adjustment of the B channel delay should be made using the procedure given in paragraph 1, above.

5. Raster Generator Alignment

Three identical raster generators are used, one for each display indicator. They are located in the scanner control unit card cage slot 6, and in the scanner logic unit slots 8 and 23 for console display units 1 and 2, respectively.

a. Adjust the unblanking gate for maximum useable display time as follows: (This adjustment interacts somewhat with adjustment b, below).

1. While observing the raster on the associated display indicator, turn the unblanking gate pot clockwise (see Fig. 68 for location) until one or more raster spots drop out.
2. Turn control ccw until all spots are again present and uniformly illuminated. (Check for all positions of the video selector switch.)

b. Adjust the raster step delay so that changes in raster spot position occur when the beam is blanked. Final criterion for adjustment is a correct, uniformly illuminated raster display, although preliminary adjustment is facilitated by viewing the z-axis and y-axis waveshapes on a two-channel oscilloscope (use co-ax tees in the lines to the display unit).

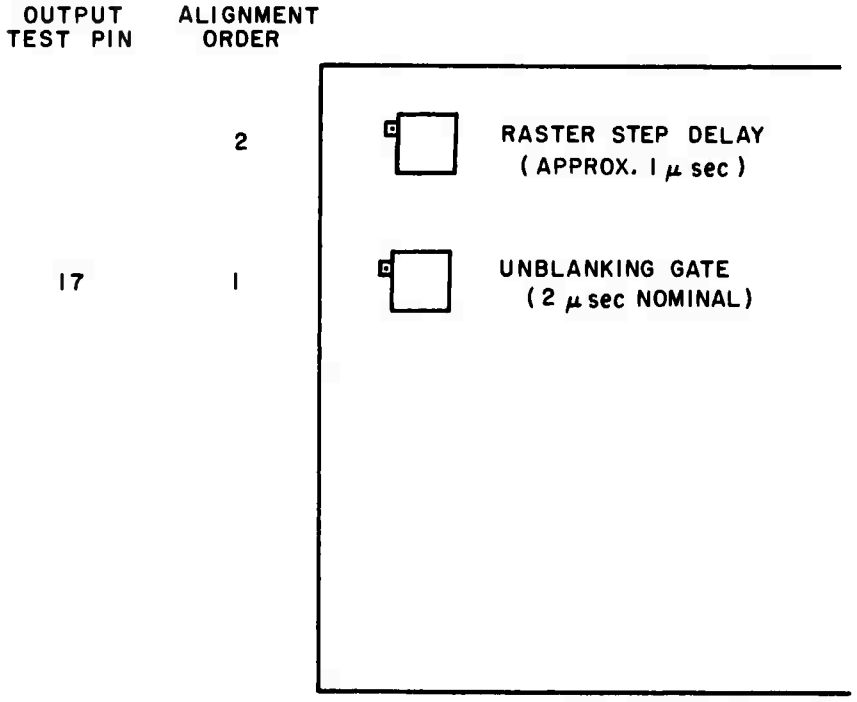


Fig. 68. Raster generator control locations.

6. Word Sync Projector Alignment

This paragraph describes mechanical alignment of the word sync projector and associated components which must be accurately positioned in order to obtain proper system operation. Since this alignment is quite tedious and critical, it should not be attempted unless the need

is clearly indicated and all other possible (and more likely) causes for malfunction have been eliminated - see Section A above. If slight misalignment of one or more adjustments are then suspected, the final alignment procedure of paragraph 1 above should first be tried before performing the following complete alignment procedure. Locations of the components are given in Figs. 15 and 17.

NOTE: It will be necessary to unbolt the scanning disc, motor, and sync assembly from the scanner baseplate and rotate it 90° clockwise for access to various components. Remove scanner cover, and use longer HV cables supplied to operate sync detectors in this position.

a. Set the even-odd splitting mirror to proper location and alignment, if required. (Splitting edge 2¼° ccw from vertically downward, facing front of disc.)

b. Remove cover from word sync projector. Loosen reticle mount clamps (L-shaped brackets holding reticle to mount). Set reticle horizontal adjustment so that centerline of reticle lies along edge of splitting mirror. (Rotate reticle to approx. position, if required, prior to this adjustment.)

c. Set up oscilloscope (multi-trace verticle plug-in, delaying sweep horizontal) to view the following waveshapes:

   (1) disc sync (TP5 of card cage) - sync all waveforms to this signal.
   (2) output of odd word sync. detector (use co-ax tee at detector)
   (3) output of even word sync. detector (use co-ax tee at detector)
   (4) A raster word sync. (TP2 of card cage).

d. Check for uniform amplitude of pulses, waveshapes (2) and (3), and adjust lamp position (and condenser if necessary) to obtain uniform amplitude.

e. Check for proper trigger level adjustment and adjust if necessary (see par. 2, above)

f. Adjust reticle rotation as follows:

   1. Raise reticle (turn vertical adjustment screw ccw) until 1st line word sync (waveshapes (2) or (3)) begin to drop out.
   2. Loosen rotation locking screws just enough to permit reticle rotation.
   3. Adjust reticle rotation (and vertical adjustment, as required) until waveshape is ½ its normal height and is of uniform height at each end of the line (i.e.,

set reticle so that outermost scanning hole just barely scans edge of reticle. To be sure of adjustment, check both waveshapes (2) and (3) in this manner. (A different vertical setting will be required for the two waveshapes.)
4. Lock rotation adjustment.
5. Turn reticle verticle adj. screw cw so that all lines are scanned, as seen by waveshapes (2) and (3).

g. Adjust projector focus.

1. Loosen 4 ¼-20 socket head cap-screws (mounting screws) on underside of projector base so that projector may be moved sideways.
2. Slide projector back and forth (keeping it against the ledge on the projector base) until baseline between pulses (most positive portion of negative waveshapes) of waveshapes (2) and (3) is as wide as possible.
3. Tighten mounting screws.

h. Adjust reticle size:

1. Loosen lens mount locking screw so that threaded lens mount can be rotated.
2. While viewing waveshapes (2), (3), and (4) rotate lens mount until even and odd word sync pulses are in proper order (i.e., odd-even-odd---) and are uniformly spaced.
3. Tighten lens mount locking screws.

i. Repeat g and h as required to obtain proper focus and size simultaneously.

j. Adjust reticle vertical position:

1. Set scope horizontal sweep so that an entire frame (i.e., 40 lines) is displayed.
2. While viewing waveshapes (2) and (3) set vertical adjustment midway between high and low settings which cause a part of the waveshapes to drop out. This is an approximate vertical setting.
3. While viewing the 1st line, waveshape (4), adjust vertical position slightly. Note that small abrupt shifts occur in the odd word sync spacing as reticle position is varied from one line to the next. Set vertical position to give most uniform spacing of even and odd word sync. pulses, waveshape (4). Recheck for other lines and shift up-or down if necessary for best spacing on all lines simultaneously.
4. Final check can be made using a magnifier to see if disc holes No. 21 and 61 actually scan top line of reticle and if disc holes No. 1 and 41 actually scan bottom line of reticle. If not, adjust reticle so that this occurs and Repeat 3 above.

7. Line, Frame, and Disc Sync Projector Alignment

The line, frame, and disc sync projector is essentially identical to the word sync projector (par. 6) except for mounting arrangement and type of reticle used. Although adjustment is far less critical than for the word sync projector because of considerably relaxed timing requirements, the following alignment should be performed only if definitely required - see Section A above.

a. Reticle rotation adjustment (preliminary)

1. Loosen rotation clamping screws
2. Adjust rotation so that top and bottom (alignment) segments of projected reticle are in alignment with the radial line scribed on edge of disc.

b. Size, Focus, and Vertical Adjustment

1. Adjust threaded lens mount for proper size of reticle on disc: i.e., size should be such that the disc sync hole and frame sync holes center in their respective reticle lines, and all scanning holes are included within the line sync portion of the reticle. NOTE: It may be necessary to adjust reticle verticle position to achieve proper positioning.
2. Check focus. If not acceptable, loosen reticle mount clamping screws and move reticle toward or away from lens for best focus. Tighten clamping screws. Repeat 1 and 2a above if clamping screws have been loosened.
3. Set vertical position for correct pattern as in 1 above.

c. Final Rotation Adjustment

1. Display line, frame, and disc sync (TP1 on card cage) on scope
2. Loosen rotation clamping screws
3. Rotate reticle to achieve uniform (6 μsec) spacing between line, frame, and disc sync. pulses
4. Tighten clamping screws.

d. Horizontal Reticle Timing Adjustment

1. Sync scope using disc sync (TP5 of card cage)
2. Display A raster word sync. on scope (TP2 of card cage).
3. Move horizontal reticle adjustment so that 1st raster word sync pulse occurs 2.5 μsec after disc sync.
4. Tighten reticle clamping screws.

e. Recheck c and d above until no further adjustment is necessary.

8. Miller Code System Alignment

General procedures for aligning the Miller code system (contained in the Ampex FR 1400 magnetic tape recorder) are given in the manual supplied by the manufacturer.[9] The procedure for aligning the encoder as given therein (as corrected) is adequate and should be followed, except that the normal scanner signals are used rather than the signal generator specified. The decoder alignment procedure, however, is not adequate for this system hence the following procedures are given.

Before any alignment of the Miller code system is attempted it is absolutely essential that all items listed in Chapter III, par. B-2-c, be checked and corrected if necessary. Recording and playback heads should be cleaned and degaussed prior to alignment, in any case. Also, circuit boards should never be removed from the recorder with power applied as this can sometimes cause the heads to become magnetized, making proper operation and alignment impossible (unless the heads are again degaussed). Make sure a high quality, thoroughly degaussed tape is used for recording during the decoder alignment.

a. Check alignment of the Miller code encoder using the procedure given in the manufacturer's manual[9] and adjust if necessary. The clock and data signals from the scanner system should be used rather than the signal generator specified, however. (NOTE: an 0101 data signal convenient for alignment can usually be obtained from the scanner system by switching off the scanner motor and allowing the disc to come to rest. If the signal is not present after the first attempt, switch on the motor momentarily and try again.)

b. If any kind of recognizable raster pattern is obtainable (using the SERIAL OUT position of the video selector) while recording a tape or playing back a pre-recorded tape known to be properly recorded (see Chap. III-B-2-c and d), the following procedure has been found to be most effective for alignment of the Miller code decoder, as well as recorder head bias, recording level (front panel gain controls) and head azimuth:

   1. With SERIAL OUT selected via the indicator video selector switch, and a tape being recorded (120 ips) using the parity check (7 bits plus parity) mode, adjust each of the following controls alternately for proper raster display and minimum error rate as previously described in Section C-1 of this appendix, i.e., Final Adjustment - General Procedure:

      (a) each adjustment of the Miller code decoder associated with the speed, and channel in use (see manufacturer's manual[9]).
      (b) head bias
      (c) input signal level
      (d) head azimuth

2. Since nearly all of the above adjustments interact, repeat 1 above until no further improvement can be obtained.

3. For playback speeds other than 120 ips, a tape pre-recorded using the parity check mode must be used. While reproducing this tape, repeat 1(a) above at the desired playback speed. (NOTE: This speed must be in agreement with the timing unit and filter installed in the low speed position of the Miller code decoder - 15 ips, at present).

c. If no recognizable raster pattern is obtainable, and the Miller code decoder is known to be misaligned (as, for example: when first installing an additional channel of Miller code electronics, or when first installing a new timing unit and filter in an existing channel) the following procedure may prove helpful:

1. Remove data input to Miller code encoder (clock only, input).
2. While monitoring the direct reproduce amplifier output (TP1 of Miller code decoder board) reduce the encoder level input (via the front panel level control) to reduce the signal level by 6 dB.
3. Peak the recording head bias (i.e., set for maximum output of the signal, step 2) and then continues turning the bias pot clockwise until the signal level drops by ½ dB.
4. Increase input level (front panel level control) to obtain maximum output signal level and then turn ccw to reduce signal level by 2 or 3 dB.
5. Reconnect signal input to encoder. Preferably use 0101 code input (see NOTE under paragraph a above).
6. With oscilloscope signal input connected to TP1 as above, but synced via the data clock, alternately adjust all Miller code decoder controls for most stable zero crossings of the "eye" pattern (i.e., multitrace ac signals) on the oscilloscope. Maintain a 2v p.p signal by adjusting reproduce level control on decoder board as required.
7. Minimum width of the ramp sample (ramp test point of decoder board) should occur simultaneous with best "eye" pattern of step 6 above.
8. Final adjustment should now be performed according to paragraph b, above.

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Step Servo Motor: DWG No. 011-017
Pulse Source: DWG No. 02283101031-0
Controller: 3 phase-1.5 Amps (Bi-directional) DWG No. 0128153312-02

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